VCRR N-Channel Enhancement Mode Power MOSFET

Description

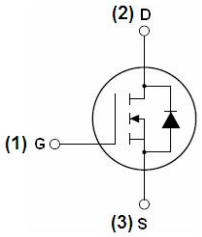
The VCRR60H10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

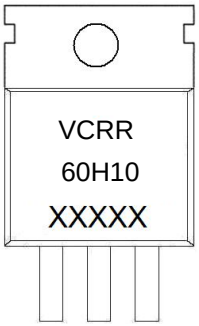
- V_{DS} =60V,I_D =100A
  $R_{DS(ON)}$ < 4.6mΩ @ V_{GS}=10V (Typ:4mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

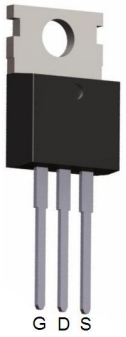
- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VCRR60H10		TO-220-3L	-	-	-

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	70	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	170	W
Derating factor		1.13	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	812	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.88	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

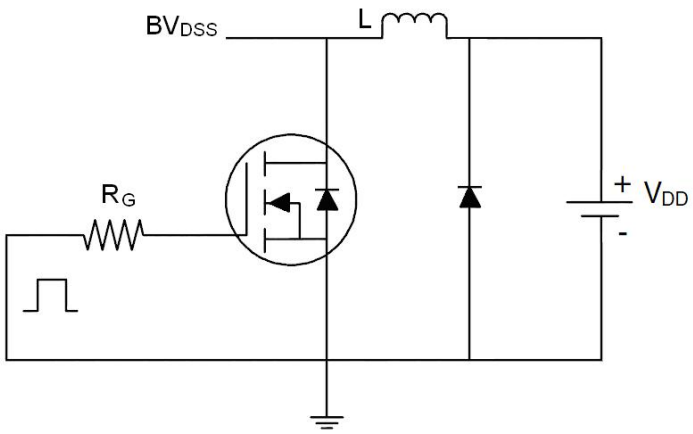
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	4	4.6	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	5200	-	PF
Output Capacitance	C_{oss}		-	410	-	PF
Reverse Transfer Capacitance	C_{rss}		-	330	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	VDD=30V,RL=1.5Ω RG=2.5Ω,VGS=10V	-	17	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=20A, V_{GS}=10V	-	100	-	nC
Gate-Source Charge	Q_{gs}		-	21	-	nC
Gate-Drain Charge	Q_{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	100	A
Reverse Recovery Time	t_{rr}	Tj=25℃,I_F=100A di/dt=100A/μs (Note3)	-		37	nS
Reverse Recovery Charge	Qrr		-		58	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

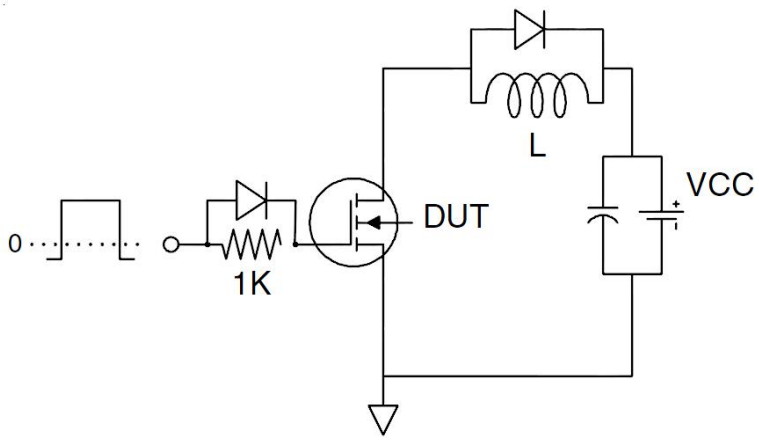
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=35V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

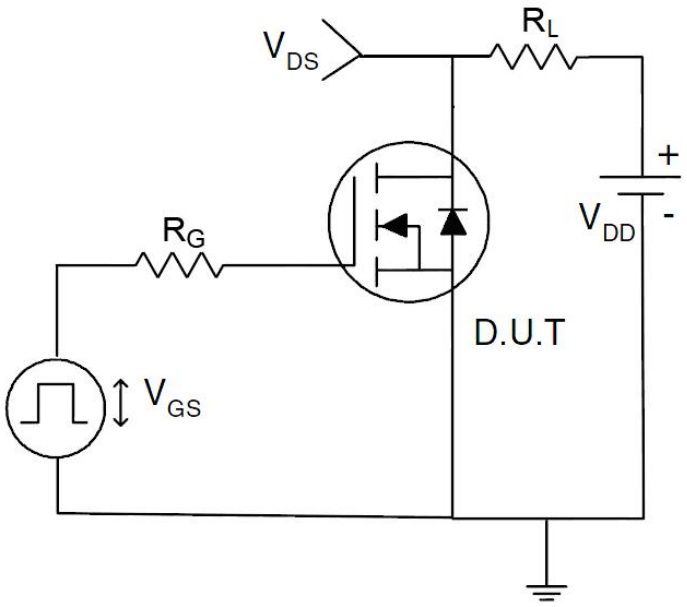
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves

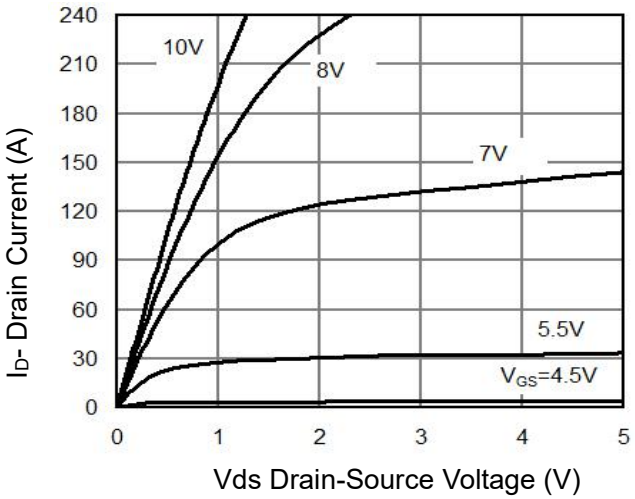


Figure 1 Output Characteristics

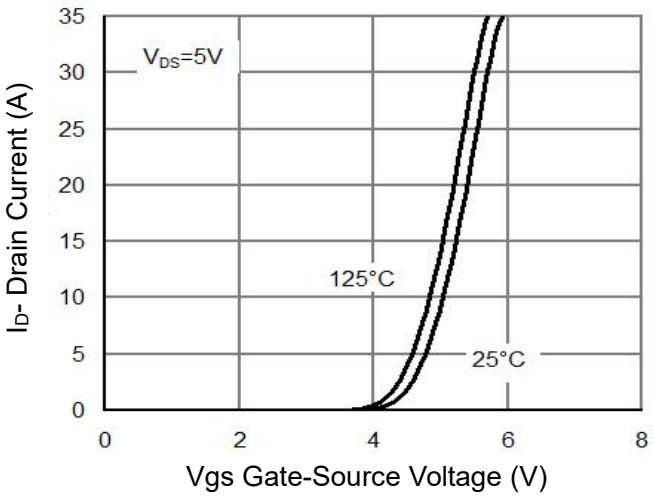


Figure 2 Transfer Characteristics

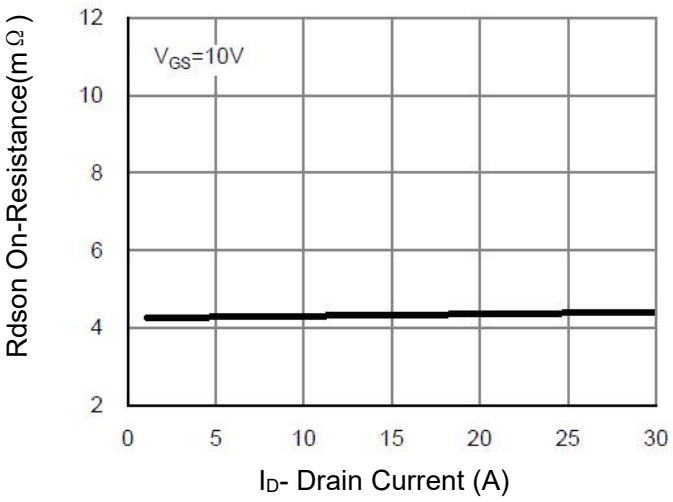


Figure 3 Rdson- Drain Current

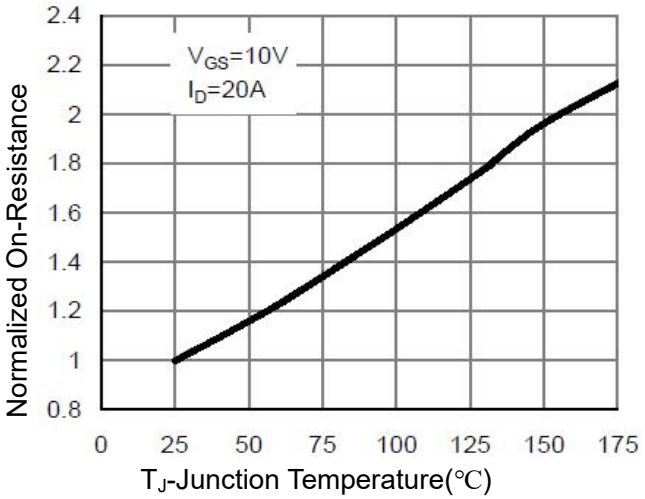


Figure 4 Rdson-Junction Temperature

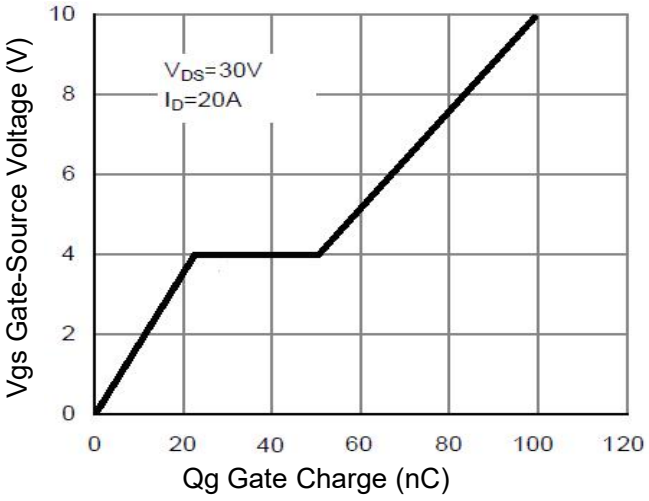


Figure 5 Gate Charge

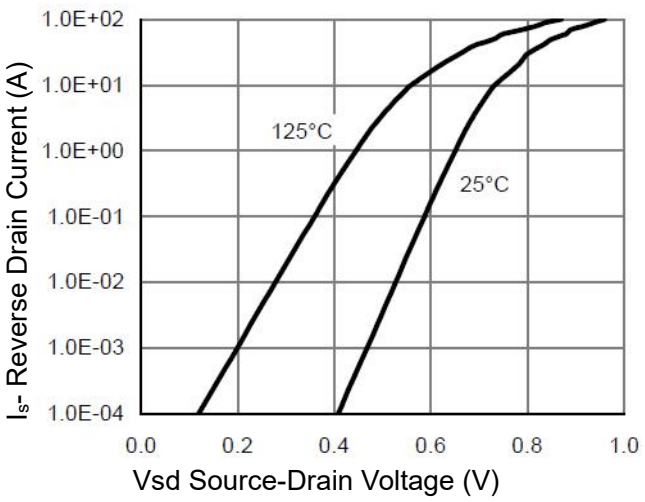


Figure 6 Source- Drain Diode Forward

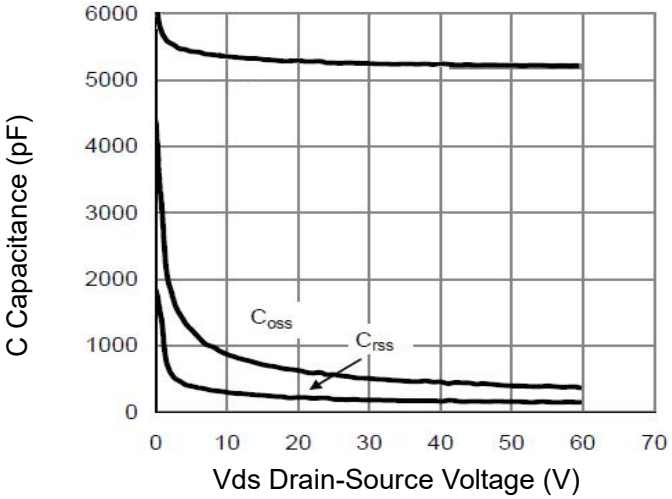


Figure 7 Capacitance vs Vds

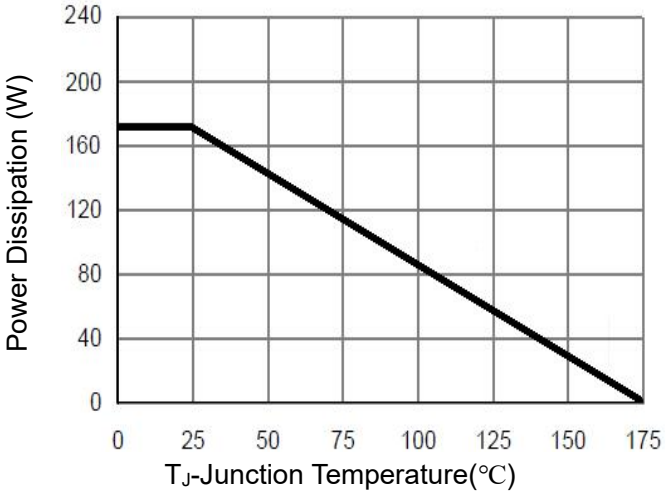


Figure 9 Power De-rating

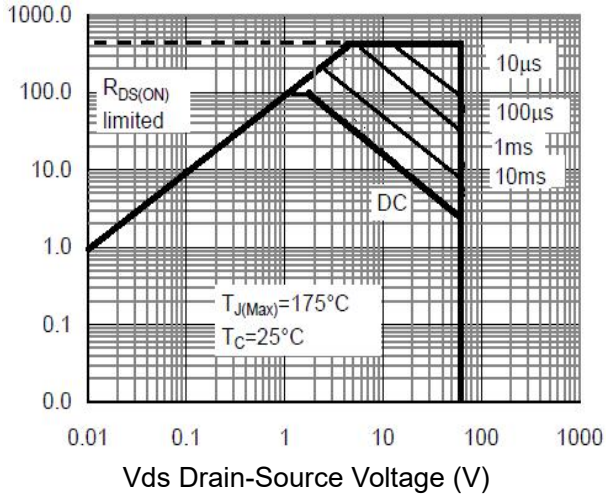


Figure 8 Safe Operation Area

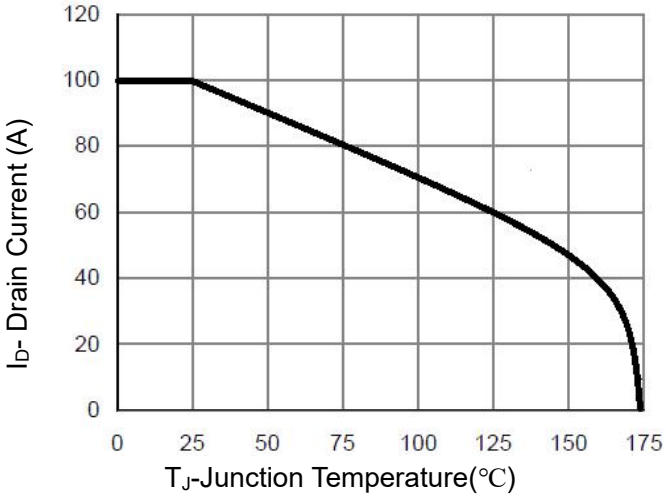


Figure 10 I_D Current De-rating

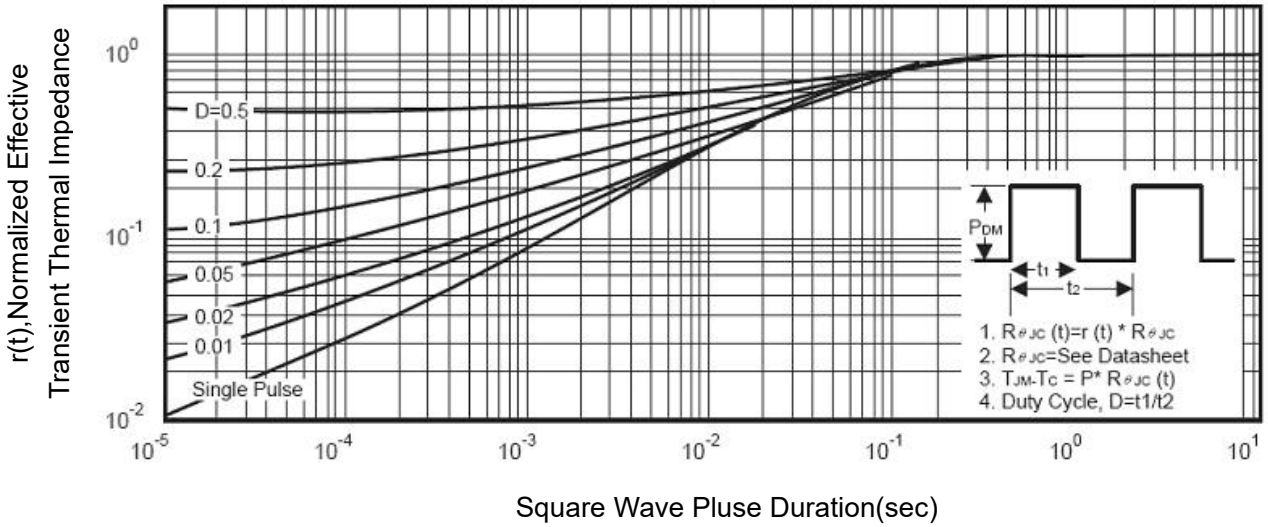
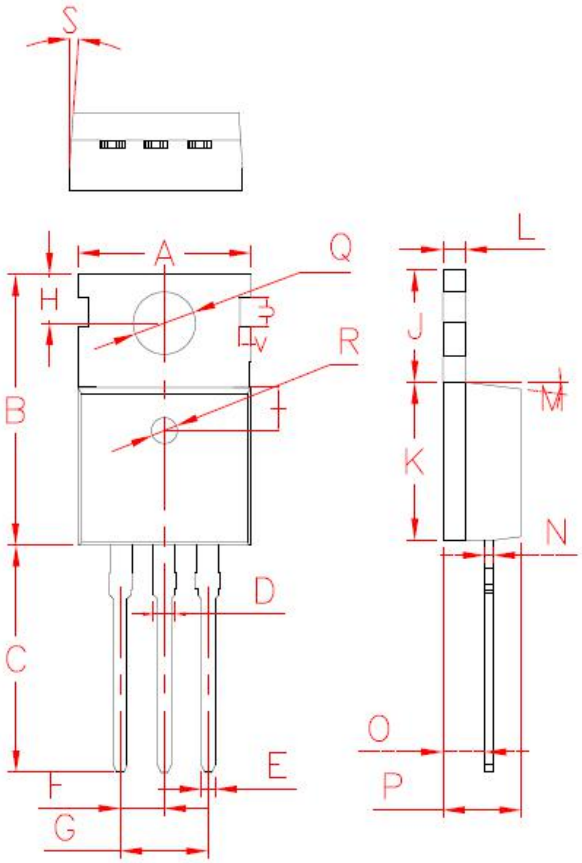


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Min	Non	Max
A	9.80	10.00	10.20
B	15.40	15.60	15.80
C	12.75	13.10	13.45
D	1.18	1.31	1.44
E	0.70	0.80	0.90
F	2.42	2.54	2.66
G	4.84	5.08	5.32
H	2.73	2.80	2.87
I	2.40	2.50	2.60
J	6.40	6.50	6.60
K	9.00	9.10	9.20
L	1.29	1.30	1.32
M	6.5°	7.0°	7.5°
N	0.48	0.50	0.56
O	2.35	2.4	2.5
P	4.4	4.5	4.7
Q	3.5	3.6	3.63
R	1.4	1.5	1.6
S	2°	2.5°	3°
U	1.65	1.75	1.85
V	0.58	0.68	0.78

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