VCRR N-ChannelEnhancement Mode Power MOSFET

Description

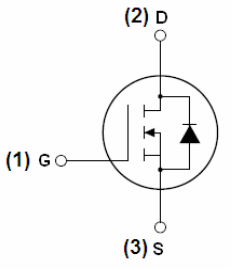
The VCRR1550 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

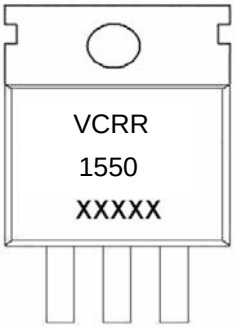
- V_{DS} =150V,I_D =50A
  $R_{DS(ON)}$ <23mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

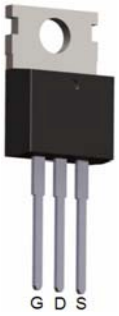
- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR1550		TO-220-3L

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	35	A
Pulsed Drain Current	I_{DM}	200	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	640	mJ

Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.68	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

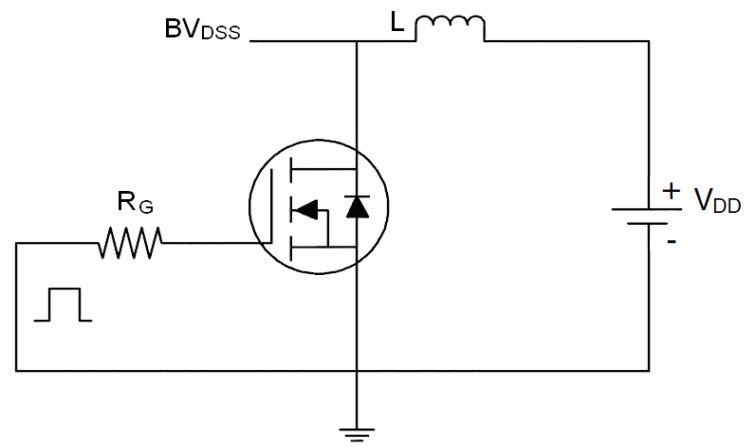
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	170	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.2	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	19.5	23	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	85	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	5300	6313.1	7800	PF
Output Capacitance	C_{oss}		-	181.2	-	PF
Reverse Transfer Capacitance	C_{rss}		-	154.3	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V,R_L=3.75Ω V_{GS}=10V,R_G=2.5Ω	-	26	-	nS
Turn-on Rise Time	t_r		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	91	-	nS
Turn-Off Fall Time	t_f		-	39	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=20A, V_{GS}=10V	-	151		nC
Gate-Source Charge	Q_{gs}		-	30		nC
Gate-Drain Charge	Q_{gd}		-	49.9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	50	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs (Note3)	-	42		nS
Reverse Recovery Charge	Qrr		-	66		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

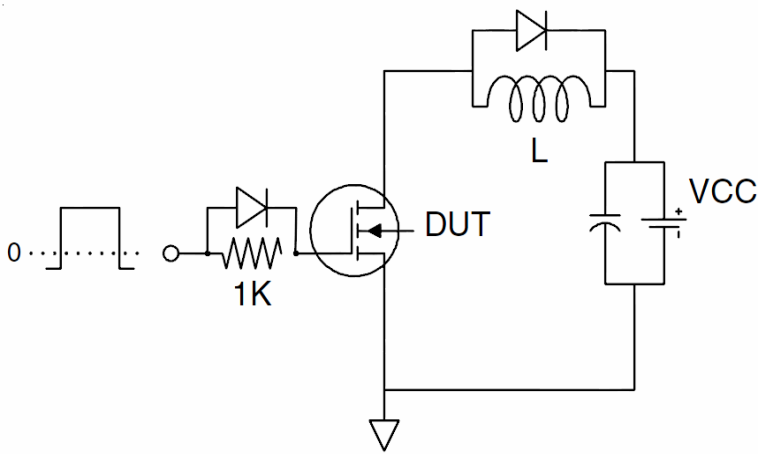
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

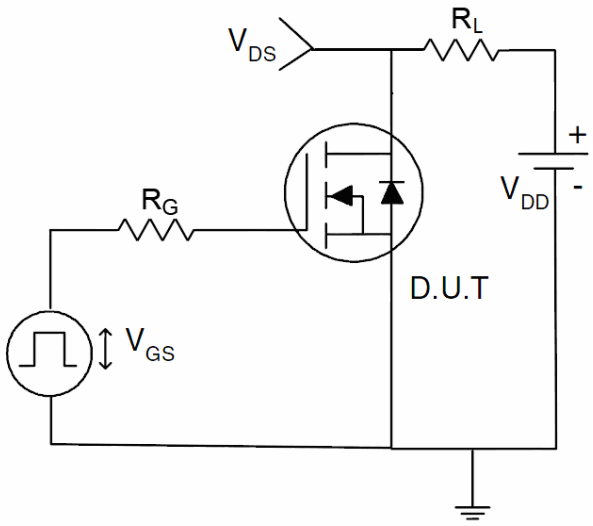
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

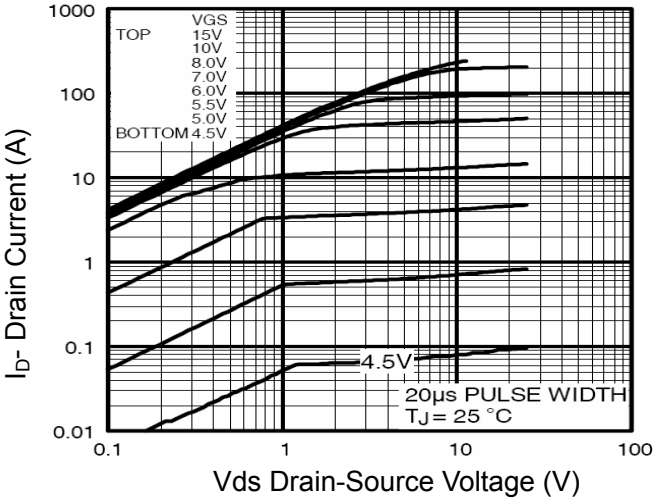


Figure 1 Output Characteristics

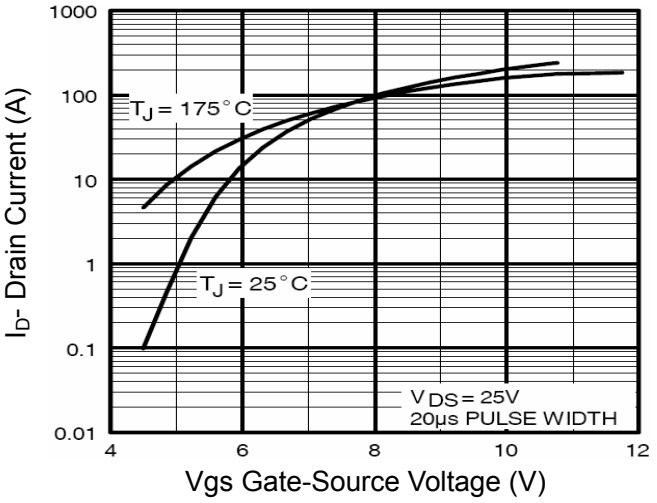


Figure 2 Transfer Characteristics

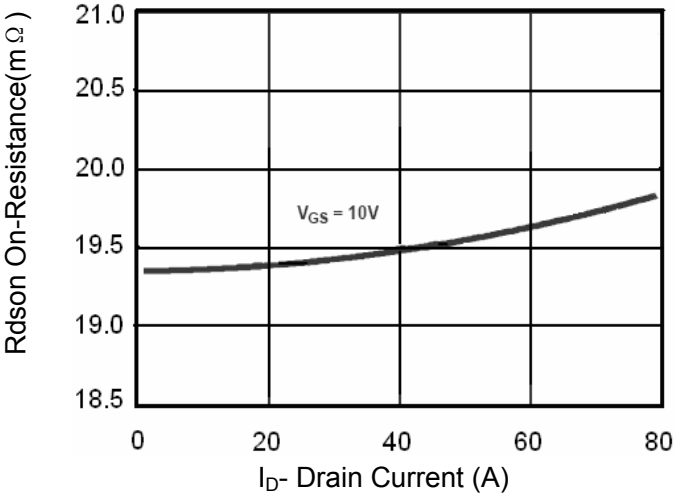


Figure 3 Rdson- Drain Current

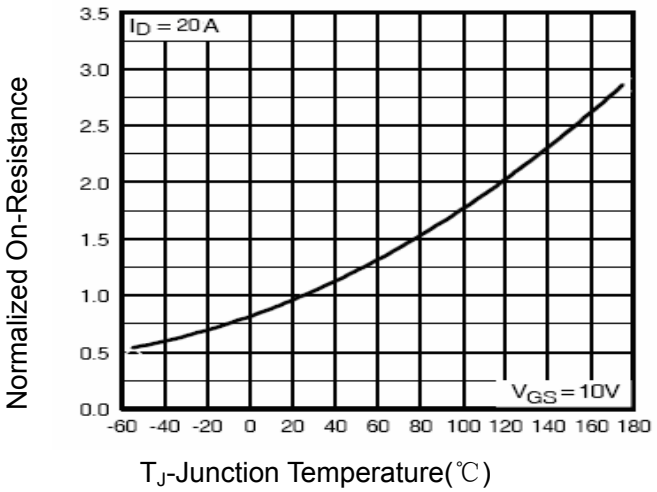


Figure 4 Rdson-JunctionTemperature

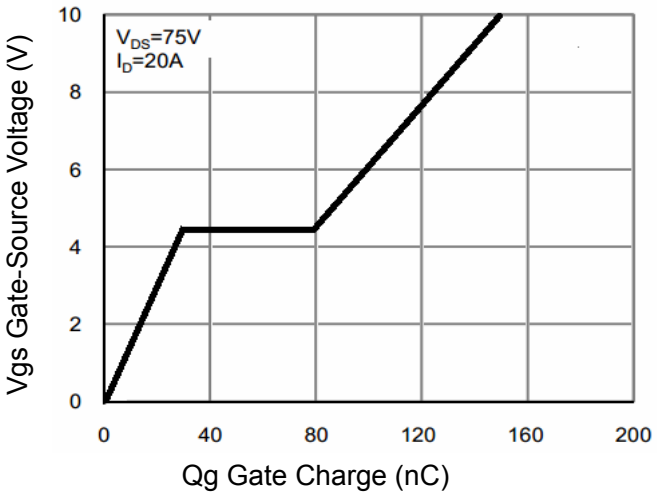


Figure 5 Gate Charge

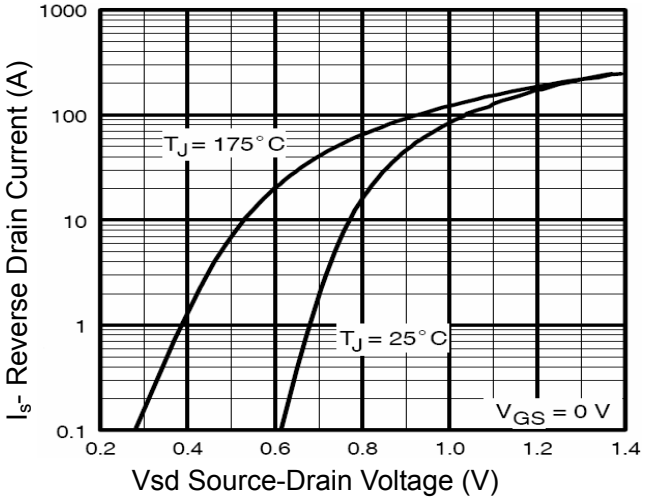


Figure 6 Source- Drain Diode Forward

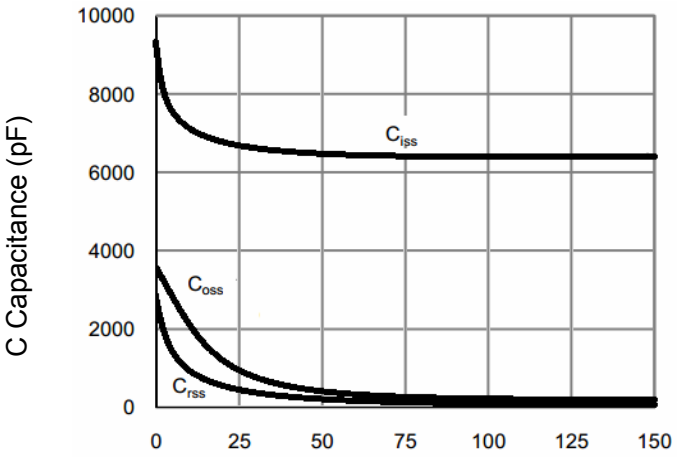


Figure 7 Capacitance vs Vds

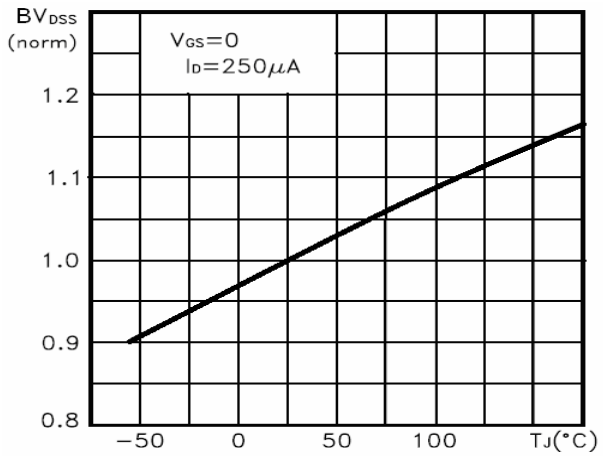


Figure 9 BV_{DSS} vs Junction Temperature

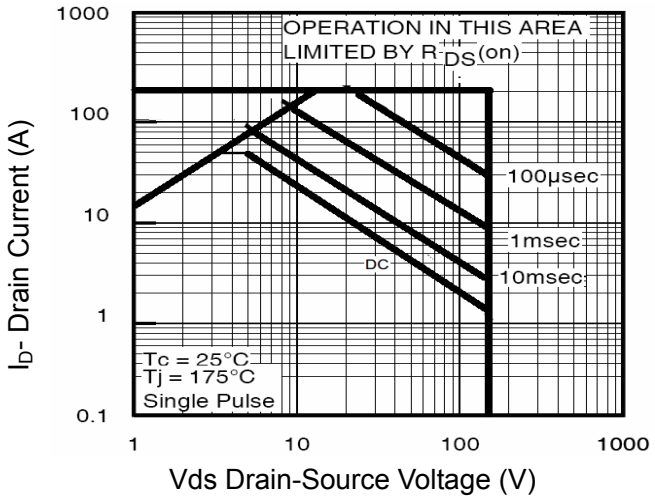


Figure 8 Safe Operation Area

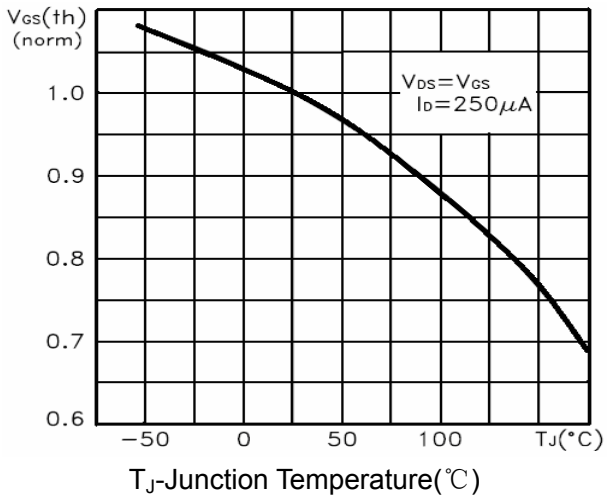


Figure 10 $V_{GS(th)}$ vs Junction Temperature

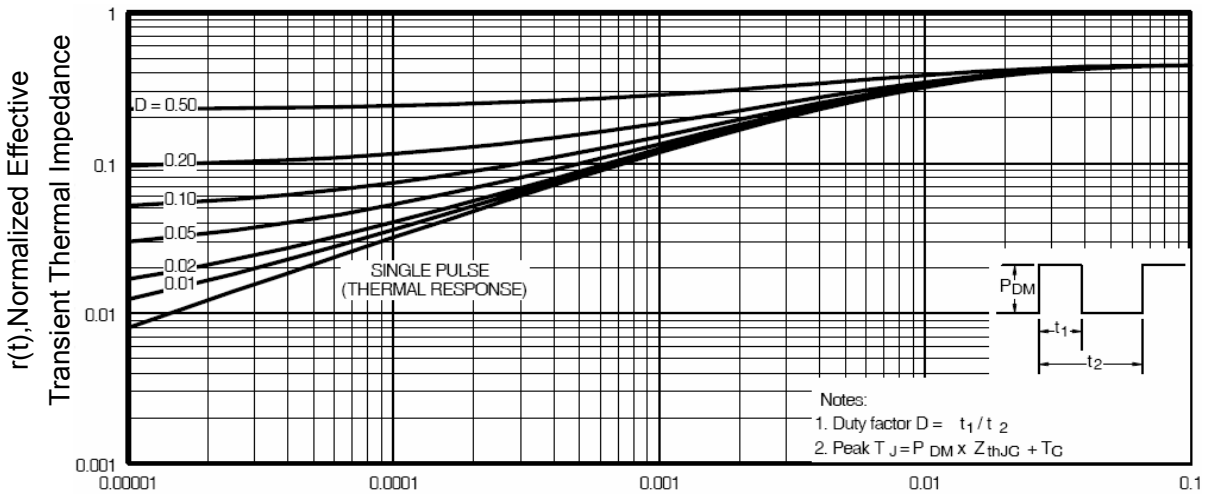
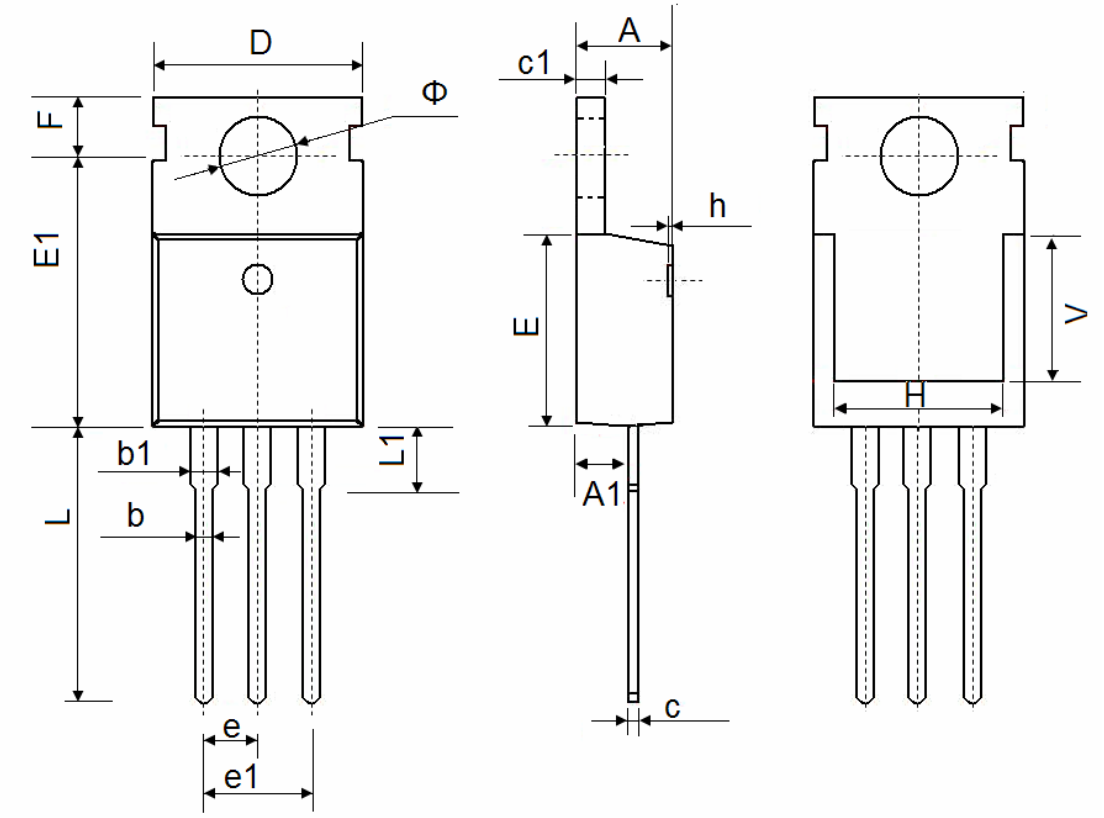


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

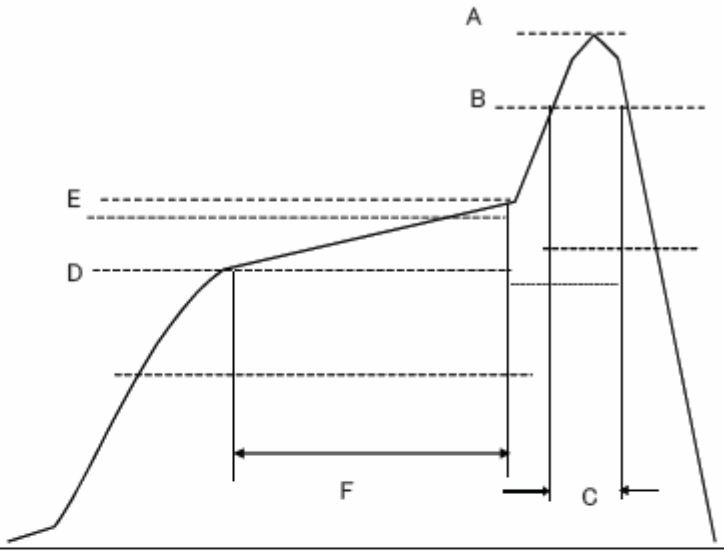
Reflow Curve

The Guarantee Letter of Parts Heat Resistance

新洁能表贴封装产品，有在以下耐热温度条件中保证的可能，建议追记到有关零件承认书的零件耐热保证项目中
(The SMD components of NCE Power have the ability of heat resistance marked below. Please add the information to corresponded items of heat resistance in Supplier Specification Submission.)

〔REFLOW温度PROFILE〕
(REFLOW TEMPERATURE PROFILE)

测试POINT：焊接部 - part表面
A: 260+5/-0 ℃ B: 217℃ C: 60~150 sec D: 150℃ E: 200℃ F: 90±10 sec



reflow条件(次数等) (Reflow condition (times))	■ 可用以上PROFILE进行3次 (can use the above profile for two times) □ 不可REFLOW (can not Reflow)		
开封后的吸湿保证条件 (Damp resistance after opening)	□无限制 (no limit) (保管条件 (store condition: 30℃ 70%RH以下) 30 ℃ 70%RH below)		
	■开封后 (after opening) 30℃ 60%RH168H→REFLOW		
手焊耐热 (Soldering iron)	350±10℃ 5+1/-0 sec	flow耐热 (flow heat-resistant)	270±3℃ 10+1/-0 sec
Pb含有状况 (Pb content status)	零件外部 (external)	■Pb完全无使用 Pb-free □Pb有使用其位置 (无铅化予定 年 月) Pb used in location (realize Pb-free year month)	
	零件内部 (inside)	□Pb完全无使用 Pb-free ■Pb有使用其位置 (内部电极含有Pb, 无铅化予定 年 月) Pb used in the inside electrodes (realize Pb-free year month)	
	电极镀层的组成 (Composition of lead cladding)	■Sn ，□Sn-Cu ，□Sn-Ag ，□Sn-Bi ，□其他(other)( ) □Sn-Pb (无铅化予定 年 月) (realize Pb-free year month)	
	无铅区分 (Pb-free manage)	□料号变更 (无铅零件料号: ABC12345) P/N changed (Pb-free P/N:) ■料号不变,自然切换 (切换时间点: 年 月 日) P/N not changed,switch naturally (switch time: year month date)	

Solder Dip	260℃ /10Sec Whole body

Attention

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