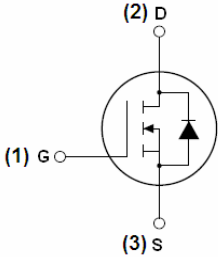
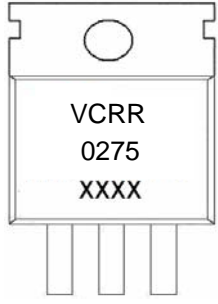



VCRR N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The VCRR0275 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in automotive applications and a wide variety of other applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● $V_{DSS} = 200V, I_D = 75A$ ● $R_{DS(ON)} < 20m\Omega @ V_{GS} = 10V$ ● Good stability and uniformity with high E_{AS} ● Special process technology for high ESD capability ● High density cell design for ultra low R_{dson} ● Fully characterized avalanche voltage and current ● Excellent package for good heat dissipation <p>Application</p> <ul style="list-style-type: none"> ● Automotive applications ● Hard switched and high frequency circuits ● Uninterruptible power supply 	<div style="text-align: center;">  <p>Schematic diagram</p>  <p>Marking and pin assignment</p>  <p>TO-220-3L top view</p> </div>
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Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR0275		TO-220-3L

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	75	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	53	A
Pulsed Drain Current ^(Note 1)	I_{DM}	300	A
Maximum Power Dissipation	P_D	360	W
Derating factor		2.4	W/ $^\circ C$
Single pulse avalanche energy ^(Note 3)	E_{AS}	1512	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 1)	$R_{\theta JC}$	0.42	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

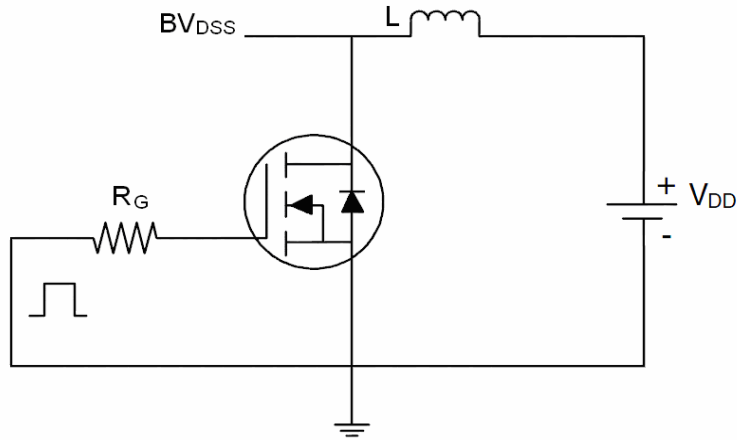
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	200	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	17.8	20	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=50V, I_D=40A$	-	79	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	6990	-	PF
Output Capacitance	C_{oss}		-	950	-	PF
Reverse Transfer Capacitance	C_{rss}		-	700	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, I_D=40A,$ $V_{GS}=10V, R_G=2.7\Omega$	-	17	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	t_f		-	22	-	nS
Total Gate Charge	Q_g	$I_D=40A, V_{DD}=100V, V_{GS}=10V$	-	140	-	nC
Gate-Source Charge	Q_{gs}		-	40	-	nC
Gate-Drain Charge	Q_{gd}		-	45	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=75A$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}C, I_F=40A$	-	136	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$ ^(Note2)	-	458	-	nC

Notes:

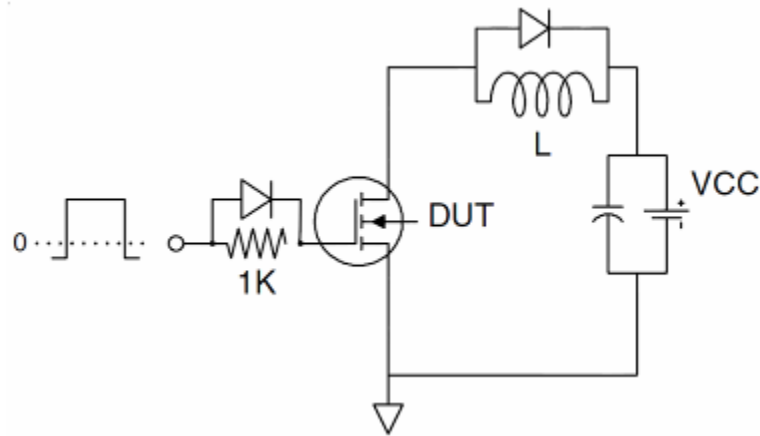
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=1mH, R_G=25\Omega, I_{AS}=55A$
4. $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^{\circ}C$

Test Circuit

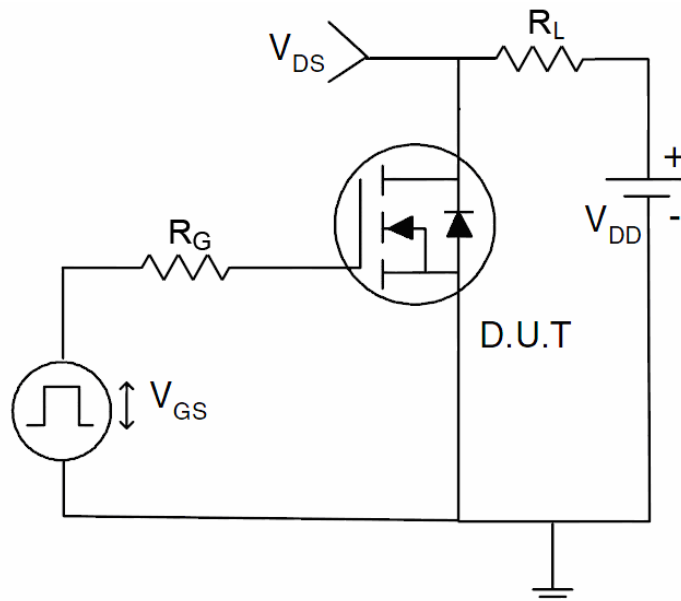
1) E_{AS} test Circuit



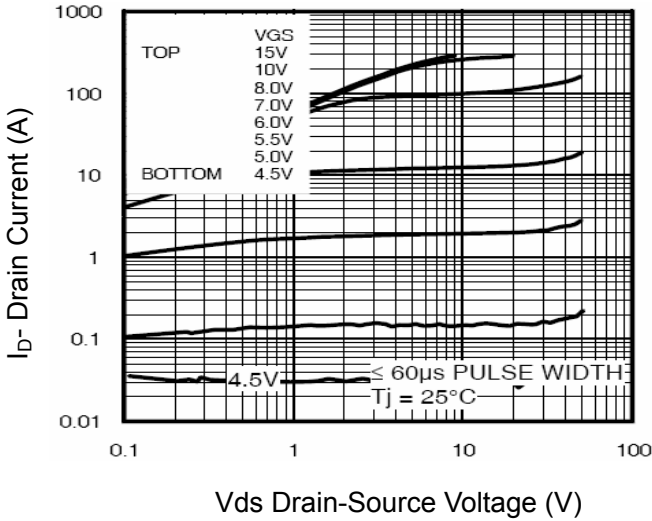
2) Gate charge test Circuit



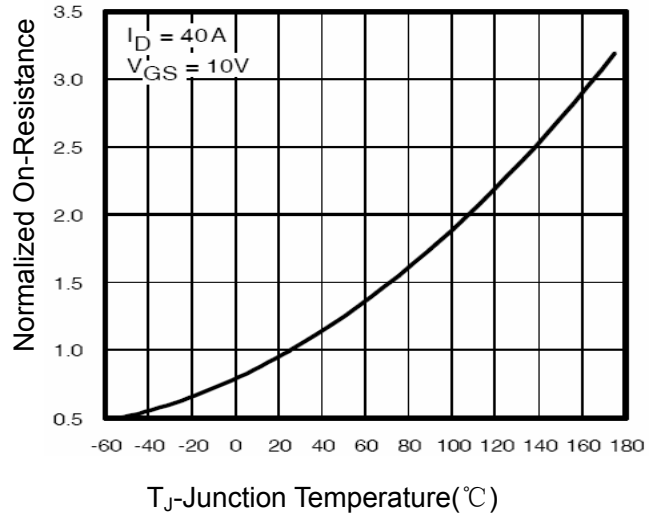
3) Switch Time Test Circuit



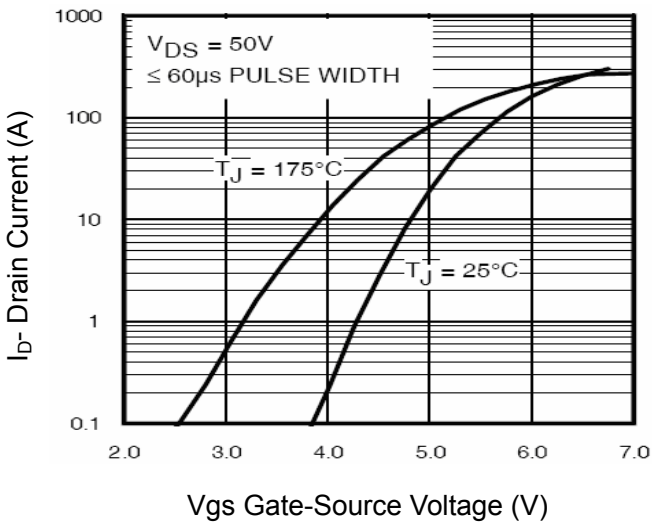
Typical Electrical and Thermal Characteristics



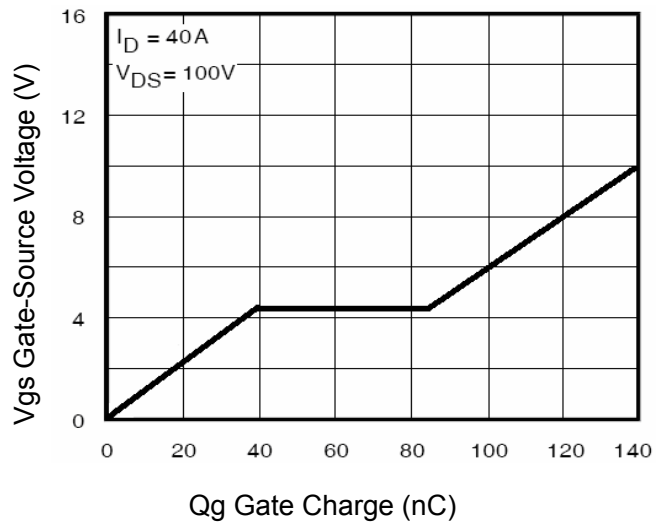
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



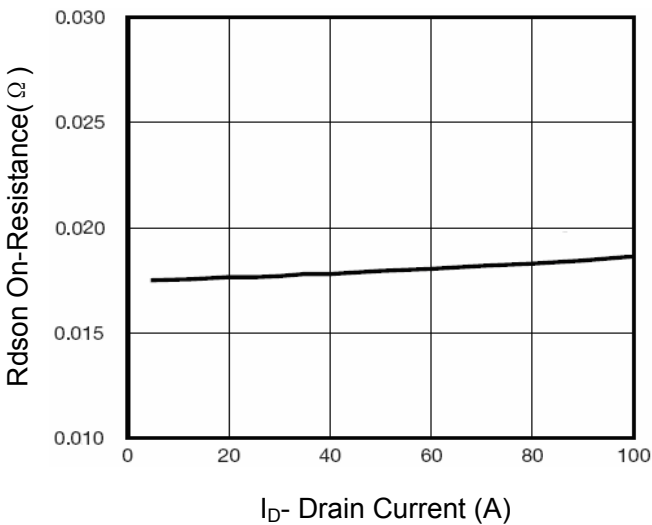
T_J-Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



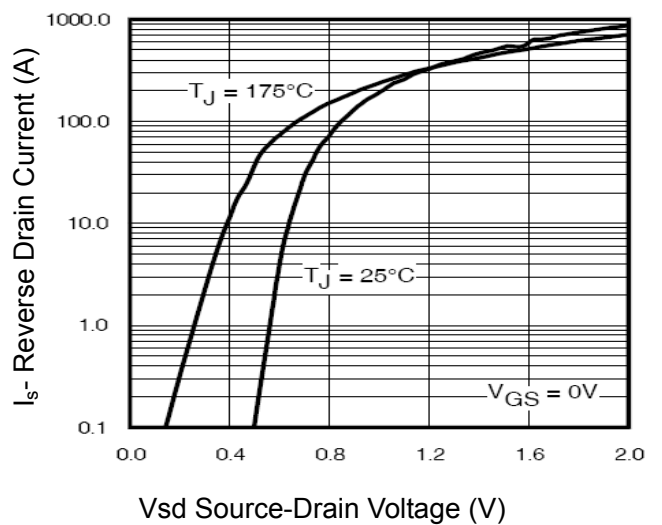
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



Qg Gate Charge (nC)
Figure 5 Gate Charge



Id- Drain Current (A)
Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

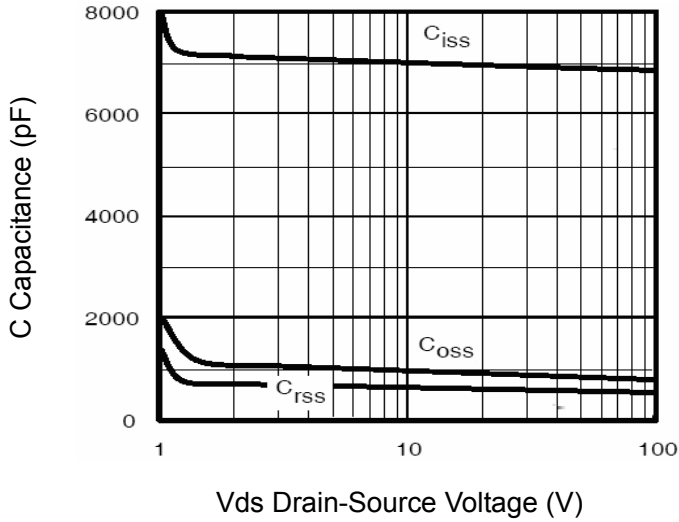


Figure 7 Capacitance vs Vds

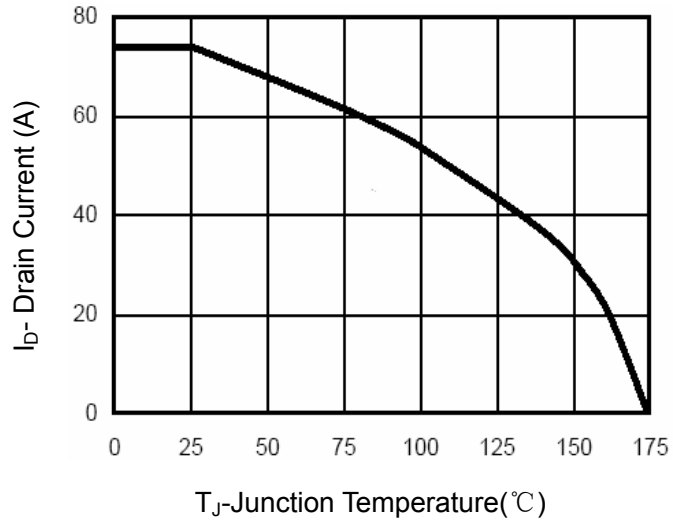


Figure 9 ID Current Derating vs Junction Temperature

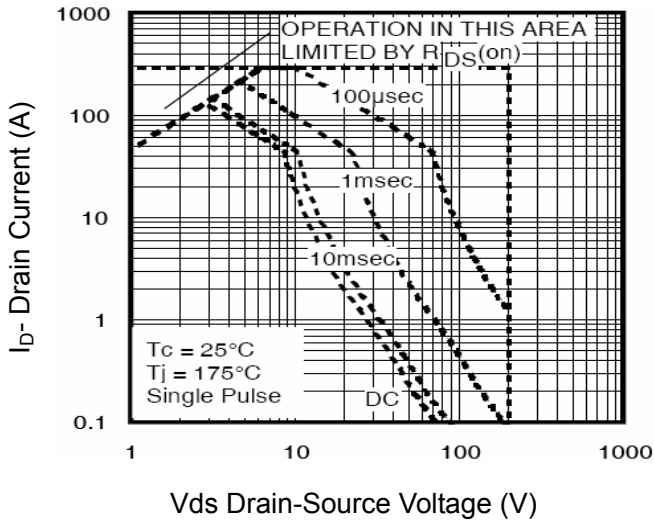


Figure 8 Safe Operation Area

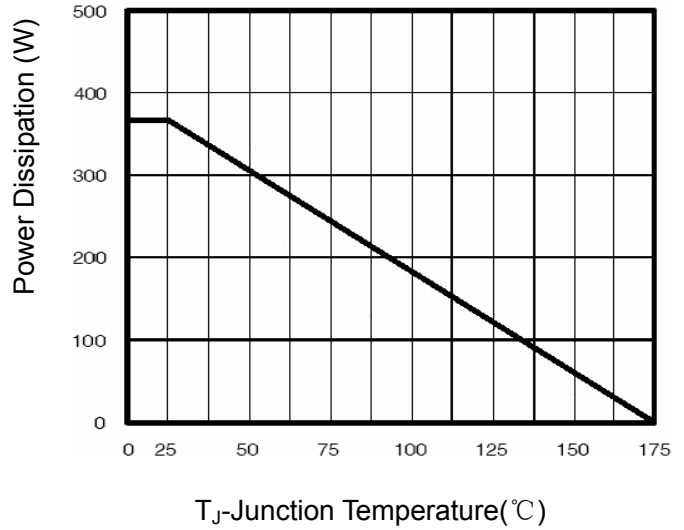


Figure 10 Power De-rating

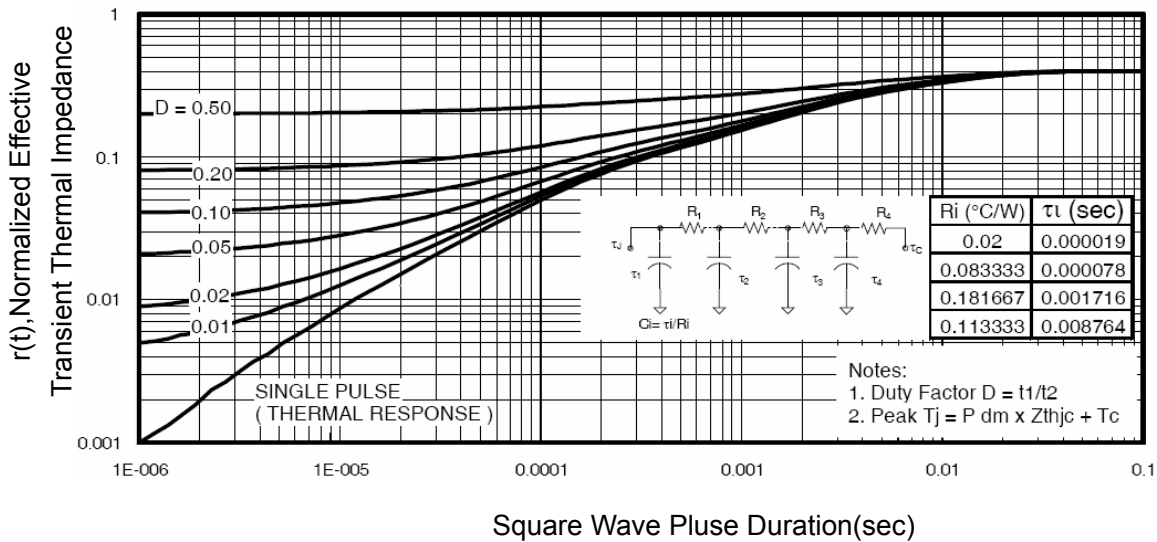
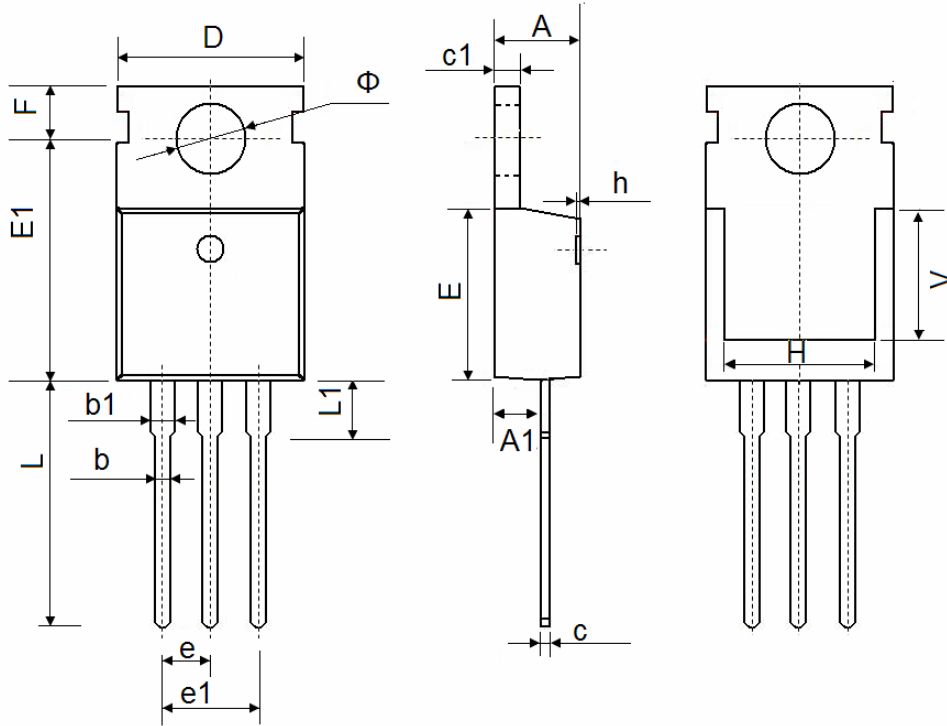


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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