

QIAOXIN N-Channel Enhancement Mode Power MOSFET

Description

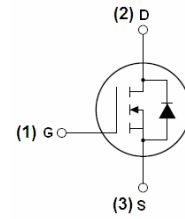
The VCRR70H10F uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

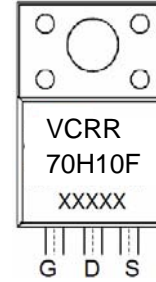
- $V_{DS} = 70V, I_D = 100A$
 $R_{DS(ON)} < 5.5 \text{ m}\Omega @ V_{GS} = 10V$ (Typ: 4.8m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Special designed for converters and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

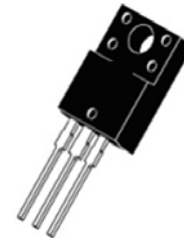
- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-220F top view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR70H10F		TO-220F

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	70	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	70.7	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.3	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	812	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.3	$^\circ\text{C}/\text{W}$
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Electrical Characteristics (T_A=25°C unless otherwise noted)

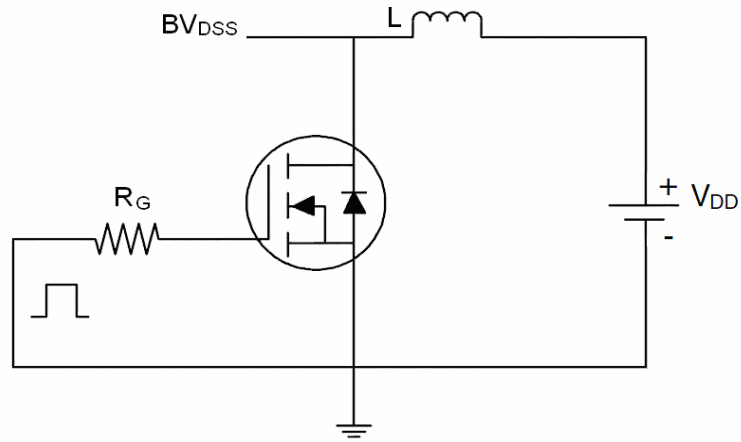
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	70	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =70V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	2.85	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	4.8	5.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	4900	-	PF
Output Capacitance	C _{oss}		-	380	-	PF
Reverse Transfer Capacitance	C _{rss}		-	290	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	VDD=35V, RL=15Ω RG=2.5Ω, VGS=10V	-	17	-	nS
Turn-on Rise Time	t _r		-	11	-	nS
Turn-Off Delay Time	t _{d(off)}		-	55	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =35V, I _D =20A, V _{GS} =10V	-	100	-	nC
Gate-Source Charge	Q _{gs}		-	21	-	nC
Gate-Drain Charge	Q _{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	100	A
Reverse Recovery Time	t _{rr}	T _j =25°C, I _F =100A di/dt=100A/μs (Note3)	-		37	nS
Reverse Recovery Charge	Q _{rr}		-		58	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

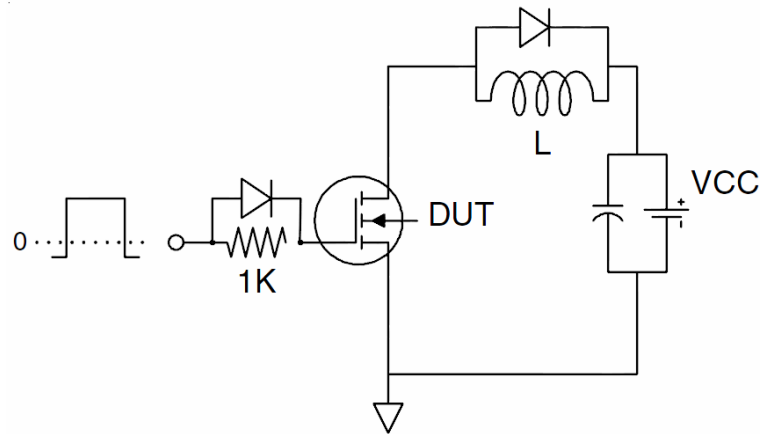
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_j=25°C, V_{DS}=35V, V_{GS}=10V, L=0.5mH, R_g=25Ω

Test Circuit

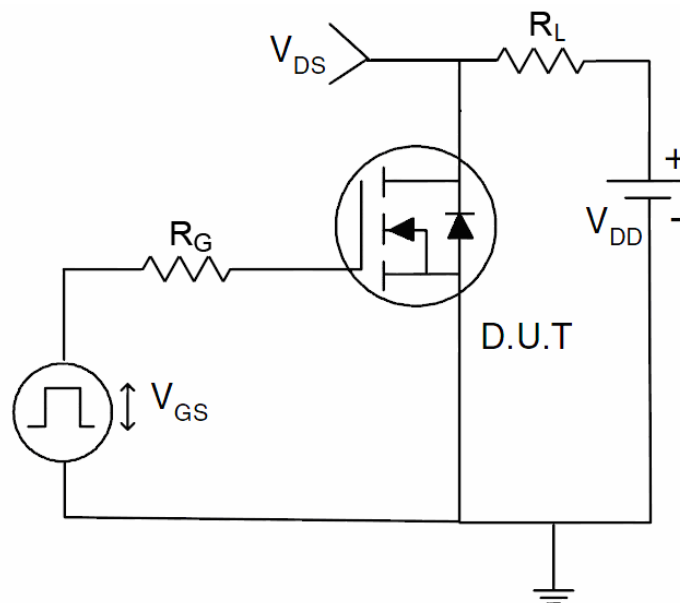
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

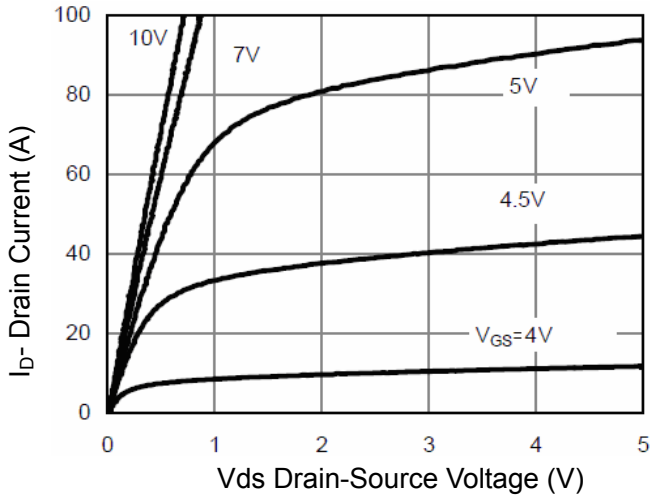


Figure 1 Output Characteristics

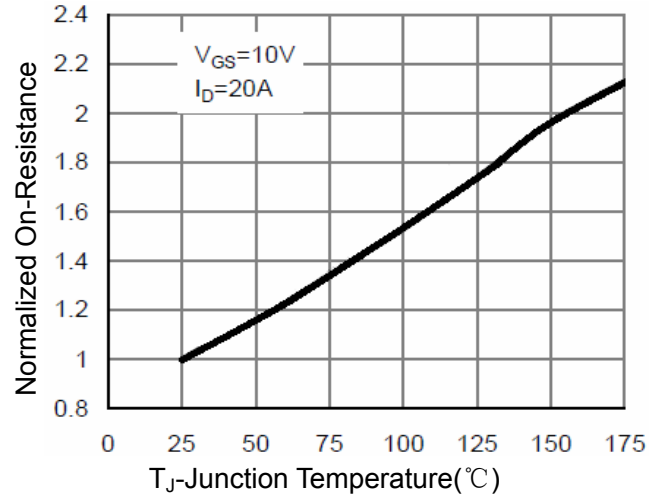


Figure 4 Rdson-Junction Temperature

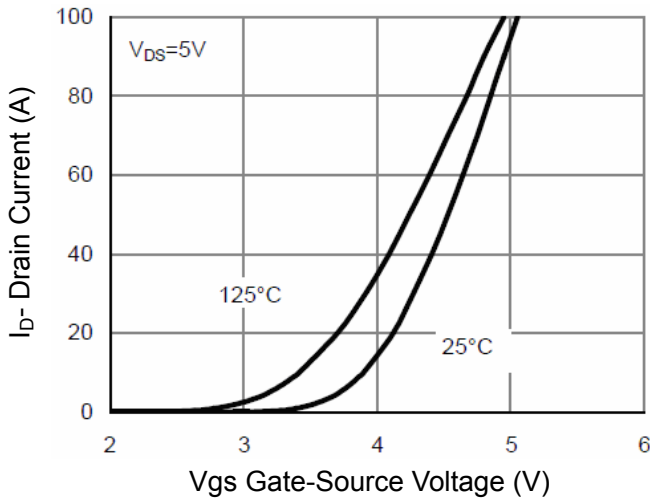


Figure 2 Transfer Characteristics

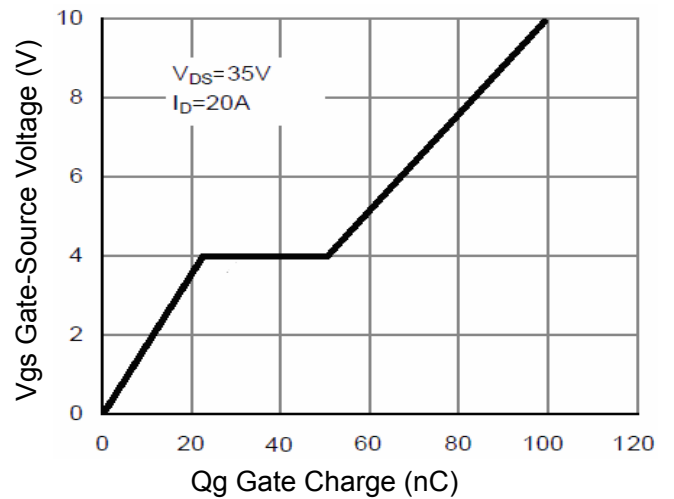


Figure 5 Gate Charge

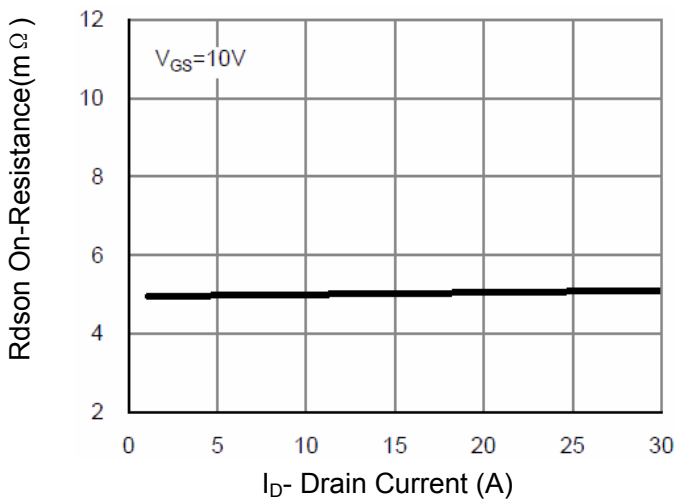


Figure 3 Rdson- Drain Current

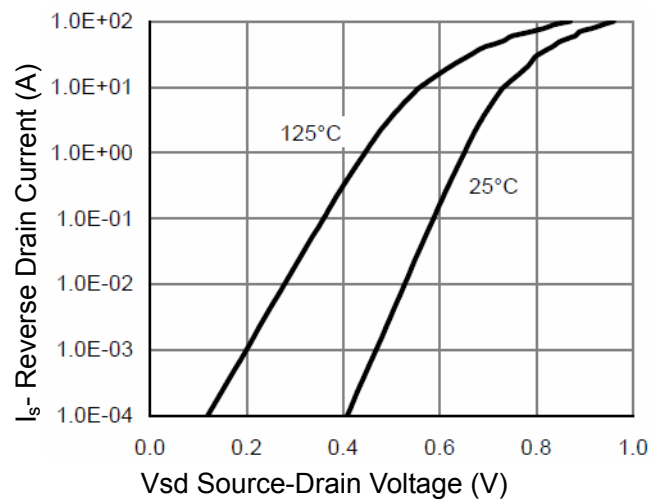


Figure 6 Source- Drain Diode Forward

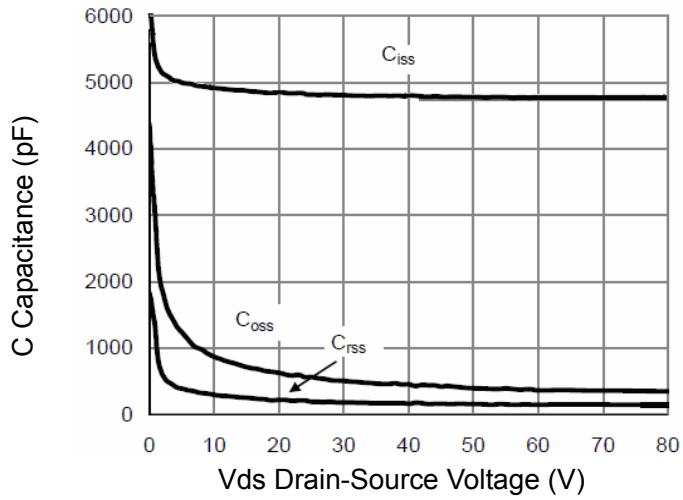


Figure 7 Capacitance vs Vds

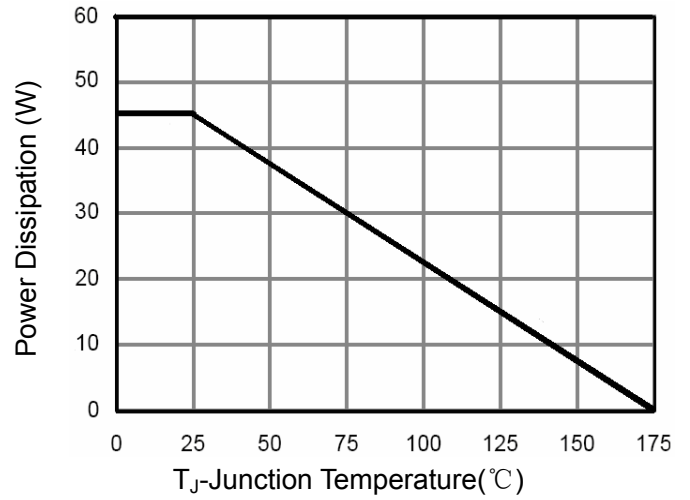


Figure 9 Power De-rating

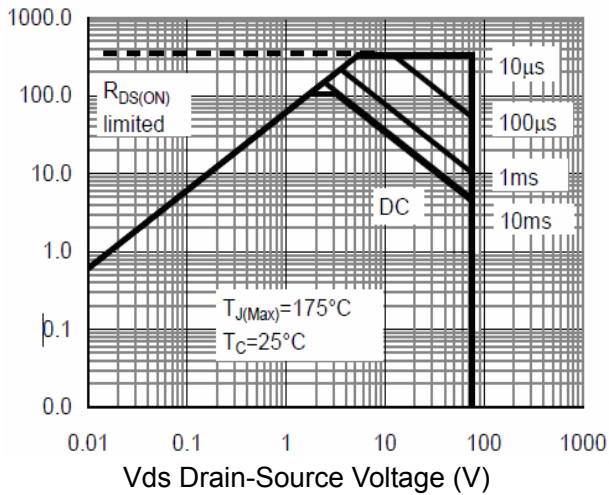


Figure 8 Safe Operation Area

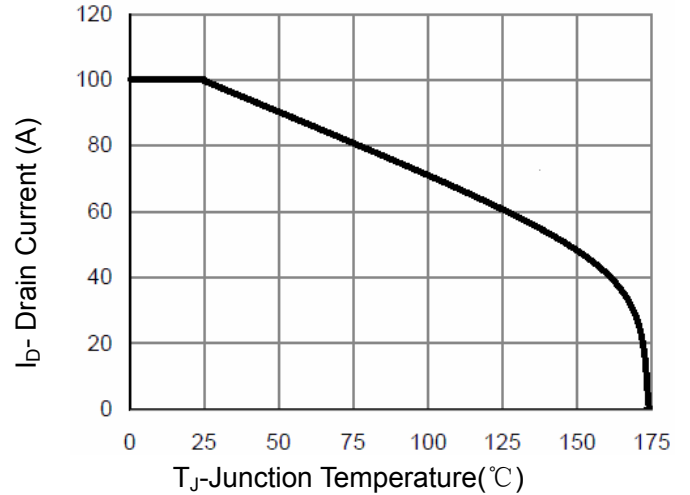


Figure 10 ID Current De-rating

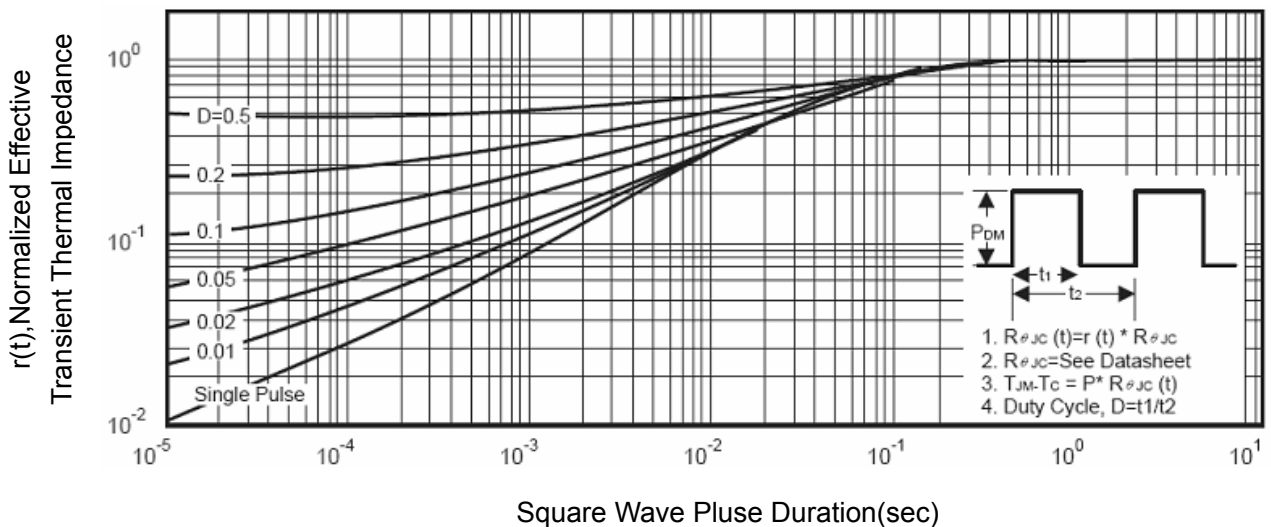
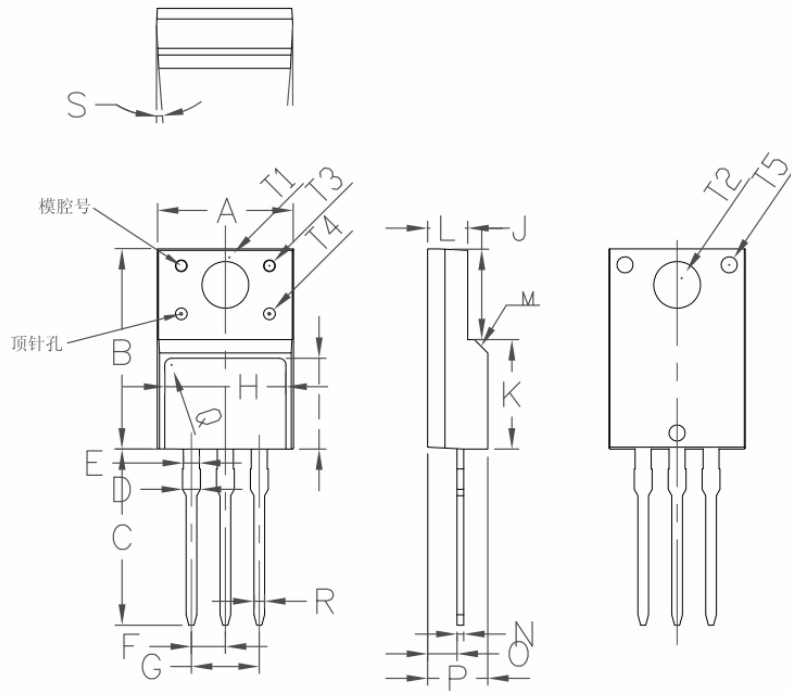


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220FPackage Information



Symbol	Min	Non	Max
A	9.96	10.16	10.36
B	15.67	15.87	16.07
C	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
H	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8.99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
O	2.15	2.35	2.55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

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