

QIAOXIN N-Channel Enhancement Mode Power MOSFET

Description

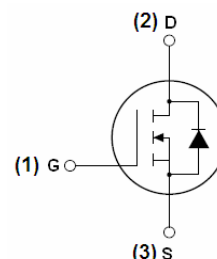
The VCRR0224AF uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

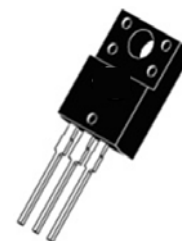
- $V_{DS} = 200V, I_D = 24A$
 $R_{DS(ON)} < 80m\Omega @ V_{GS} = 10V$ (Typ: 62m Ω)
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



TO-220F top view

Package Marking and Ordering Information

| Device Marking | Device | Device Package |
|----------------|--------|----------------|
| VCRR0224AF | | TO-220F |

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---------------------|------------|------------|
| Drain-Source Voltage | V_{DS} | 200 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | I_D | 24 | A |
| Drain Current-Continuous ($T_C = 100^\circ C$) | $I_D (100^\circ C)$ | 16.5 | A |
| Pulsed Drain Current | I_{DM} | 100 | A |
| Maximum Power Dissipation | P_D | 45 | W |
| Single pulse avalanche energy ^(Note 5) | E_{AS} | 250 | mJ |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55 To 175 | $^\circ C$ |

Thermal Characteristic

| | | | |
|---|-----------------|------|--------------|
| Thermal Resistance, Junction-to-Ambient ^(Note 2) | $R_{\theta JA}$ | 3.33 | $^\circ C/W$ |
|---|-----------------|------|--------------|

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

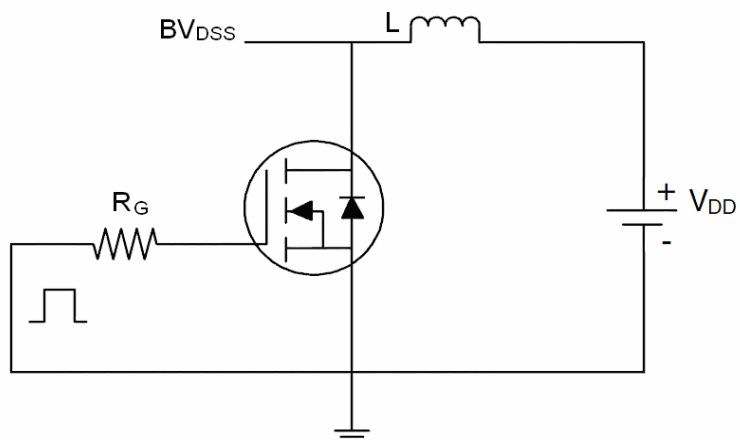
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------|---|-----|------|-----------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 200 | 220 | - | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=200V, V_{GS}=0V$ | - | - | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| On Characteristics (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | 1.5 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}=10V, I_D=15A$ | - | 62 | 80 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS}=10V, I_D=15A$ | 30 | - | - | S |
| Dynamic Characteristics (Note4) | | | | | | |
| Input Capacitance | C_{ISS} | $V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$ | | 4200 | | PF |
| Output Capacitance | C_{OSS} | | | 163 | | PF |
| Reverse Transfer Capacitance | C_{RSS} | | | 75 | | PF |
| Switching Characteristics (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}=100V, I_D=15A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$ | - | 10 | - | nS |
| Turn-on Rise Time | t_r | | - | 18 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 22 | - | nS |
| Turn-Off Fall Time | t_f | | - | 5 | - | nS |
| Total Gate Charge | Q_g | $V_{DS}=100V, I_D=15A,$ $V_{GS}=10V$ | | 60 | | nC |
| Gate-Source Charge | Q_{gs} | | | 19 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 17 | | nC |
| Drain-Source Diode Characteristics | | | | | | |
| Diode Forward Voltage (Note 3) | V_{SD} | $V_{GS}=0V, I_S=15A$ | - | - | 1.2 | V |
| Diode Forward Current (Note 2) | I_S | - | - | - | 24 | A |
| Reverse Recovery Time | t_{rr} | $T_J = 25^{\circ}\text{C}, I_F = 15A$ $di/dt = 100A/\mu s$ (Note3) | - | 90 | - | nS |
| Reverse Recovery Charge | Q_{rr} | | - | 300 | - | nC |

Notes:

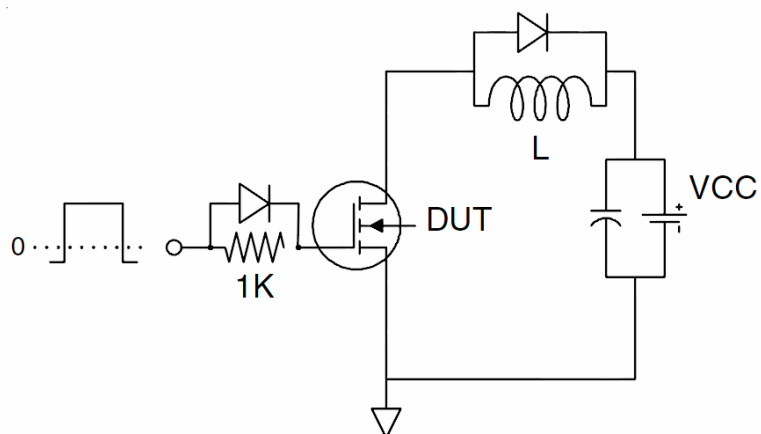
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

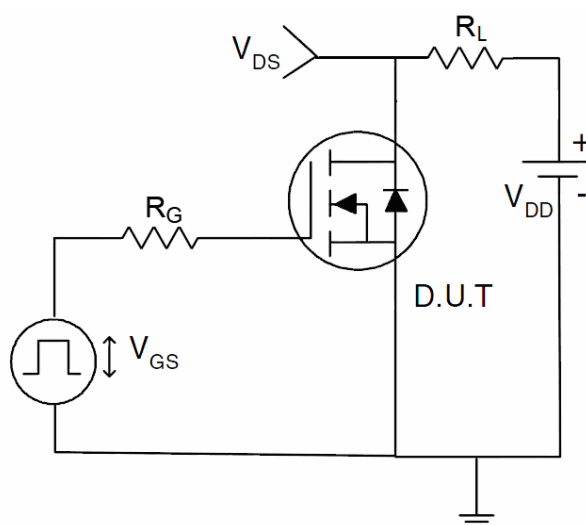
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

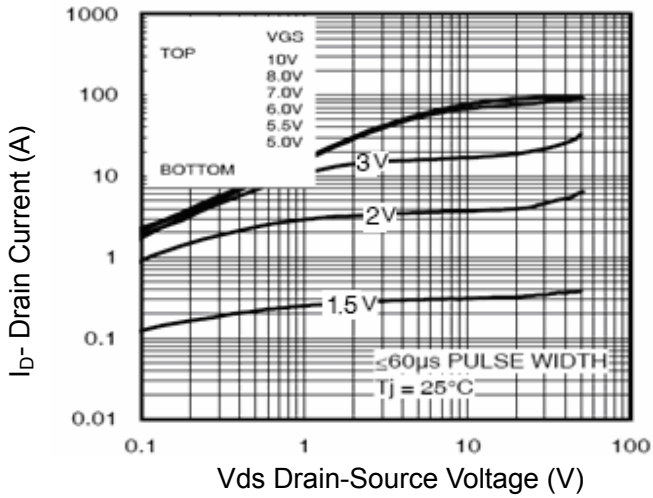


Figure 1 Output Characteristics

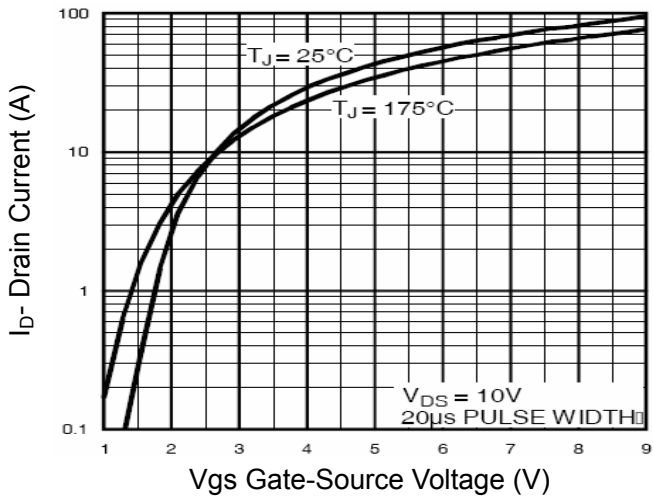


Figure 2 Transfer Characteristics

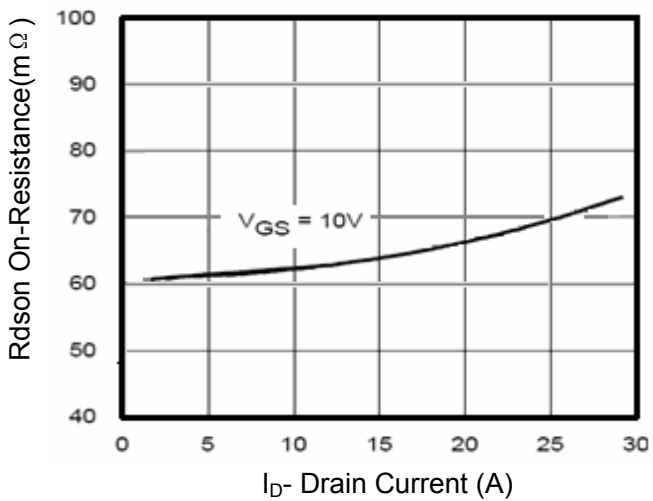


Figure 3 $R_{DS(on)}$ - Drain Current

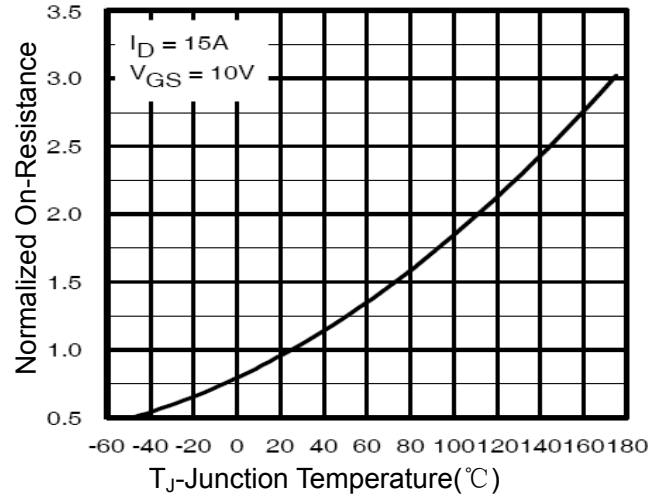


Figure 4 $R_{DS(on)}$ -Junction Temperature

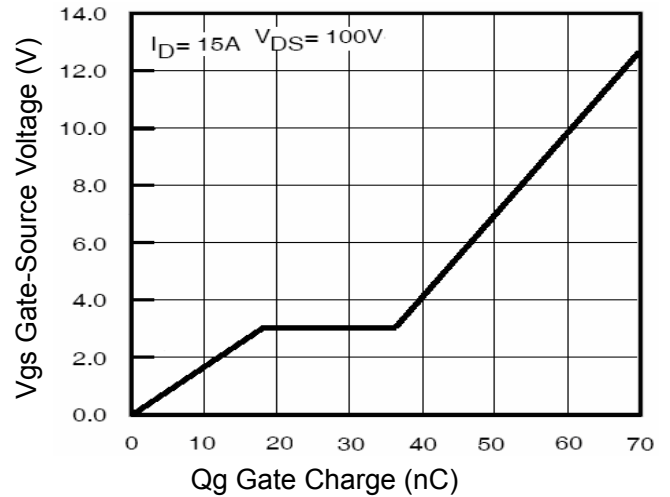


Figure 5 Gate Charge

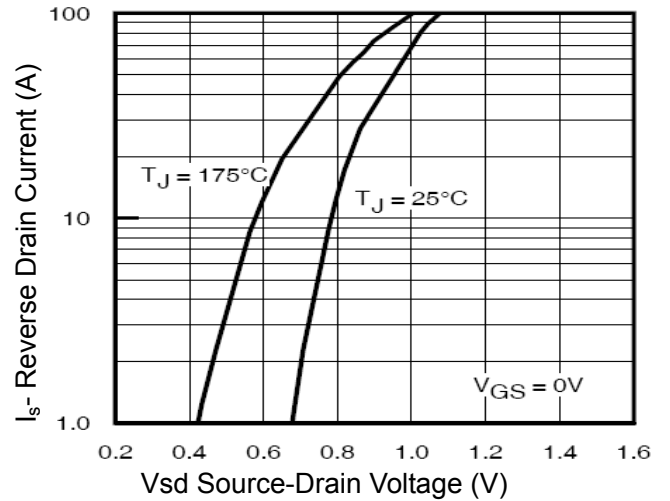


Figure 6 Source- Drain Diode Forward

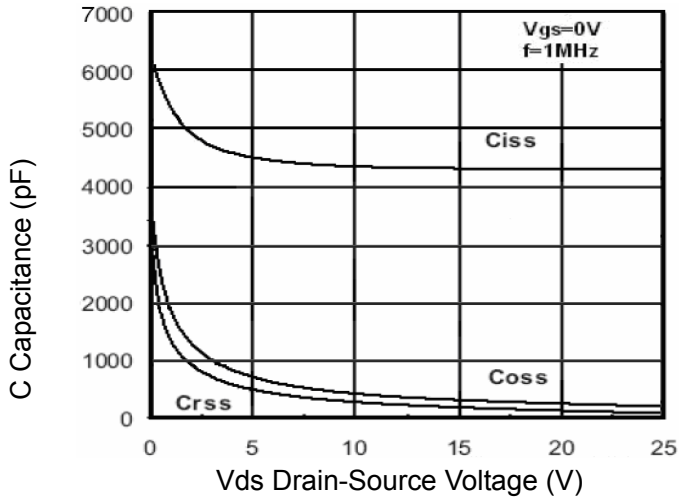


Figure 7 Capacitance vs Vds

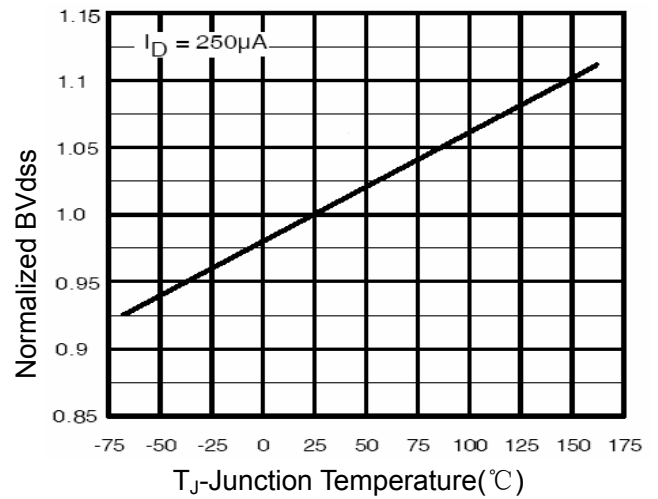


Figure 9 BV_{DSS} vs Junction Temperature

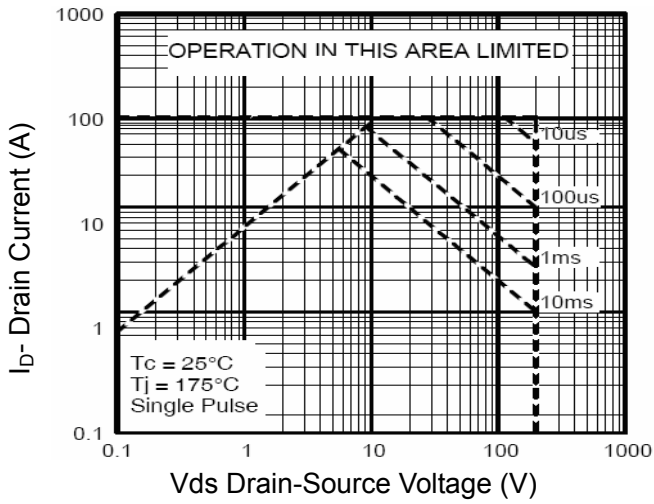


Figure 8 Safe Operation Area

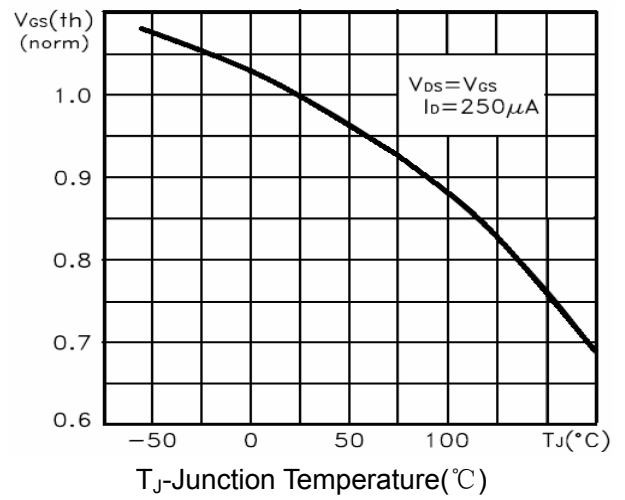


Figure 10 $V_{GS(th)}$ vs Junction Temperature

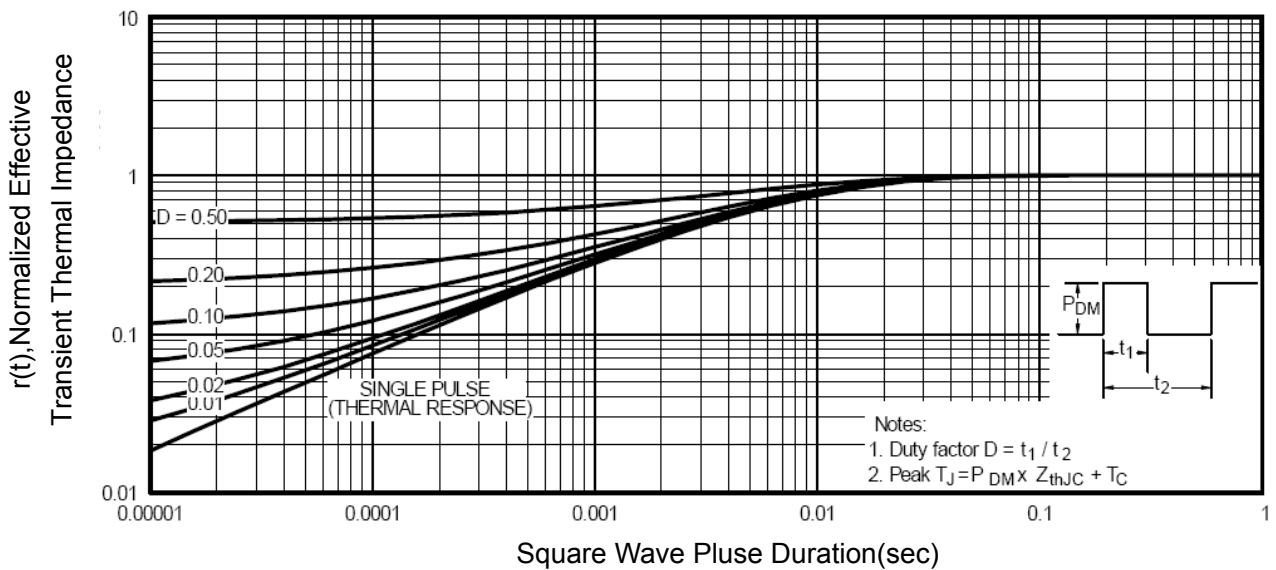
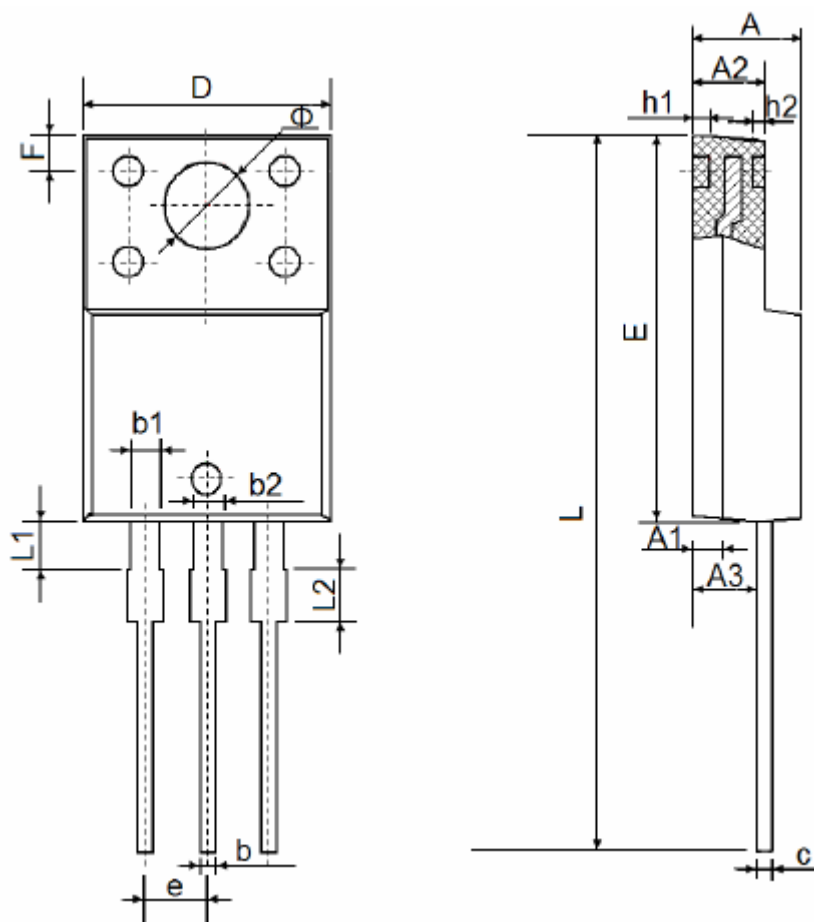


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220F Package Information



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|--------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 4.300 | 4.700 | 0.169 | 0.185 |
| A1 | 1.300REF | | 0.051REF | |
| A2 | 2.800 | 3.200 | 0.110 | 0.126 |
| A3 | 2.500 | 2.900 | 0.098 | 0.114 |
| b | 0.500 | 0.750 | 0.020 | 0.030 |
| b1 | 1.100 | 1.350 | 0.043 | 0.053 |
| b2 | 1.500 | 1.750 | 0.059 | 0.069 |
| c | 0.500 | 0.750 | 0.020 | 0.030 |
| D | 9.960 | 10.360 | 0.392 | 0.408 |
| E | 14.800 | 15.200 | 0.583 | 0.598 |
| e | 2.540TYP. | | 0.100TYP | |
| F | 2.700REF | | 0.106REF | |
| Φ | 3.500REF | | 0.138REF | |
| h1 | 0.800REF | | 0.031REF | |
| h2 | 0.500REF | | 0.020REF | |
| L | 28.000 | 28.400 | 1.102 | 1.118 |
| L1 | 1.700 | 1.900 | 0.067 | 0.075 |
| L2 | 1.900 | 2.100 | 0.075 | 0.083 |

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