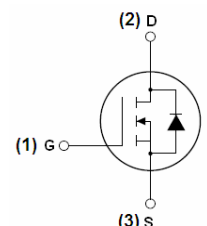




QIAOXIN N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The VCRR40H30D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● $V_{DS} = 40V$, $I_D = 300A$ $R_{DS(ON)} < 1.8m\Omega @ V_{GS} = 10V$ ● High density cell design for ultra low R_{dson} ● Fully characterized avalanche voltage and current ● Good stability and uniformity with high E_{AS} ● Excellent package for good heat dissipation ● Special process technology for high ESD capability <p>Application</p> <ul style="list-style-type: none"> ● Power switching application ● Hard switched and high frequency circuits ● Uninterruptible power supply 	<div style="text-align: center;">  <p>Schematic diagram</p>  <p>Marking and pin assignment</p>  <p>TO-263-2L top view</p> </div>
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Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR40H30D		TO-263-2L

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	300	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	212	A
Pulsed Drain Current	I_{DM}	840	A
Maximum Power Dissipation	P_D	350	W
Derating factor		2.33	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	2500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.43	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

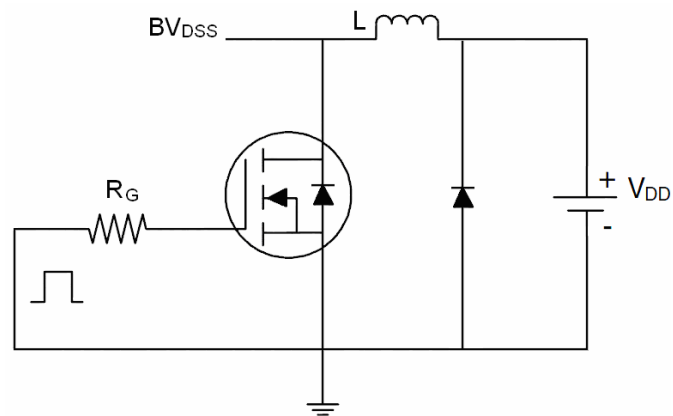
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=150A$	-	1.4	1.8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=150A$	-	100	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	11635	-	PF
Output Capacitance	C_{OSS}		-	1360	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	1229	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=15\Omega,$ $R_G=2.5\Omega, V_{GS}=10V$	-	42	-	nS
Turn-on Rise Time	t_r		-	41	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	150	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	$I_D=150A, V_{DD}=20V, V_{GS}=10V$	-	249	-	nC
Gate-Source Charge	Q_{GS}		-	40	-	nC
Gate-Drain Charge	Q_{gd}		-	80	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=150A$	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	300	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 300A$ $di/dt = 100A/\mu\text{s}$ (Note3)	-	55		nS
Reverse Recovery Charge	Q_{rr}		-	180		nC

Notes:

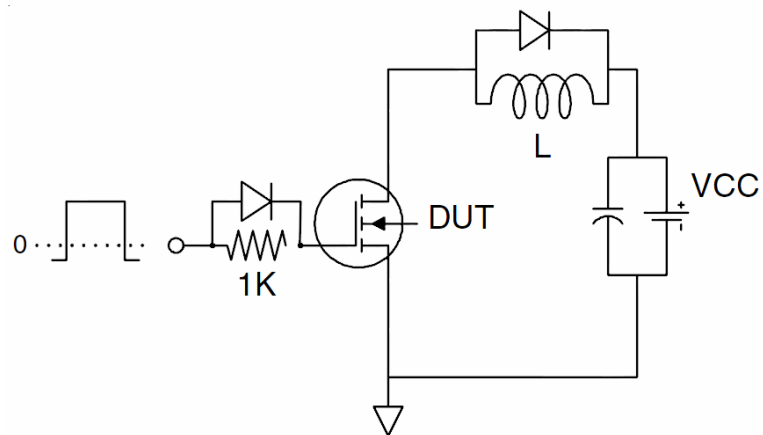
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Test circuit

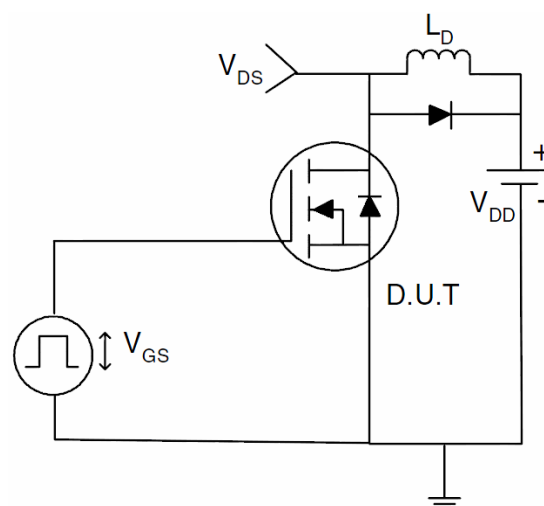
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

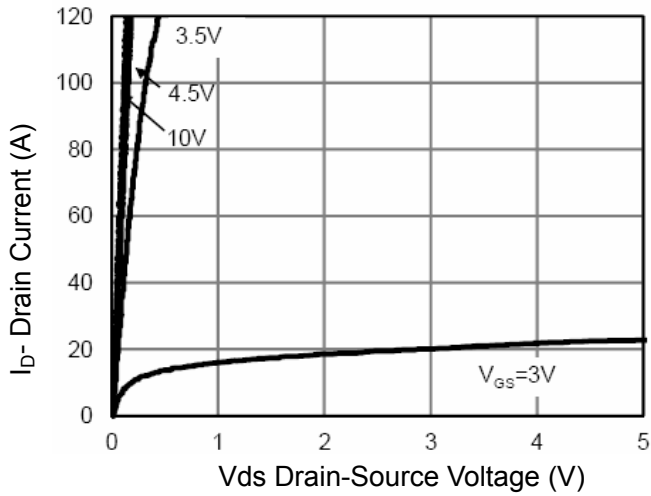


Figure 1 Output Characteristics

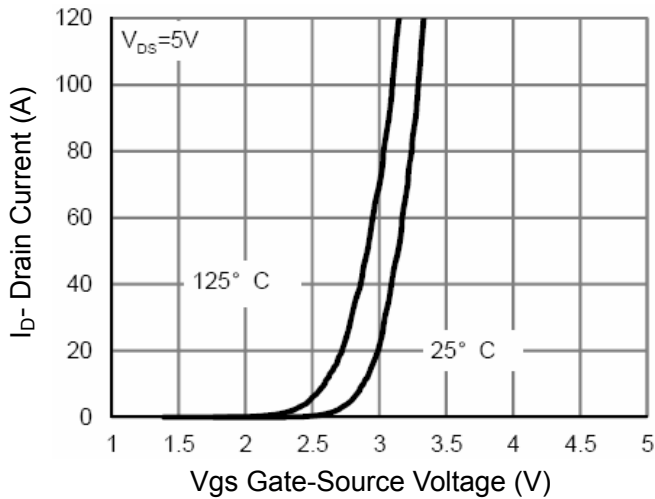


Figure 2 Transfer Characteristics

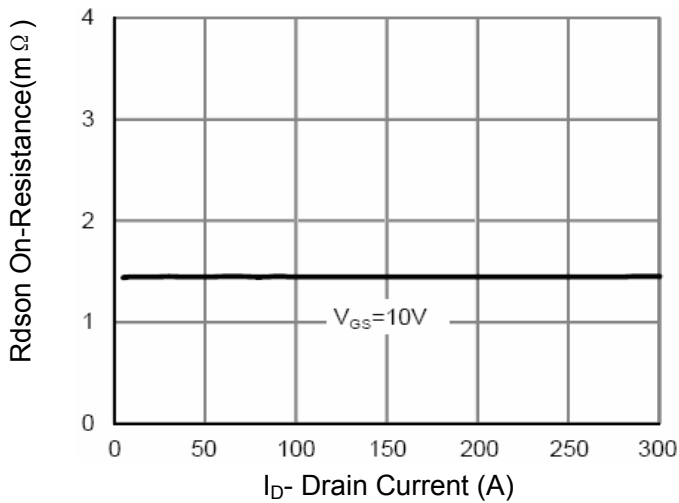


Figure 3 Rdson- Drain Current

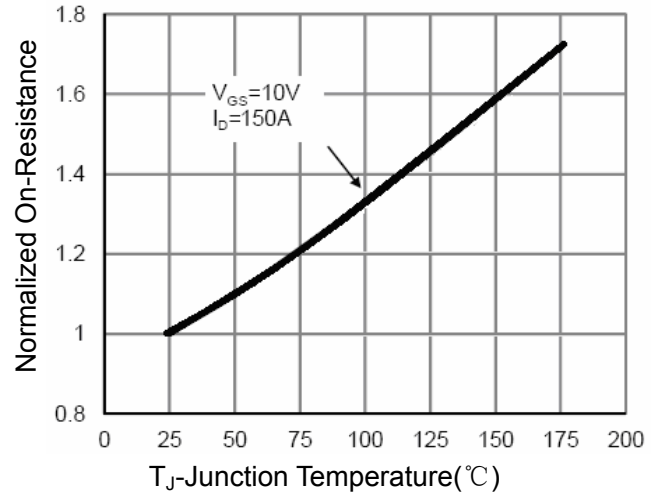


Figure 4 Rdson-Junction Temperature

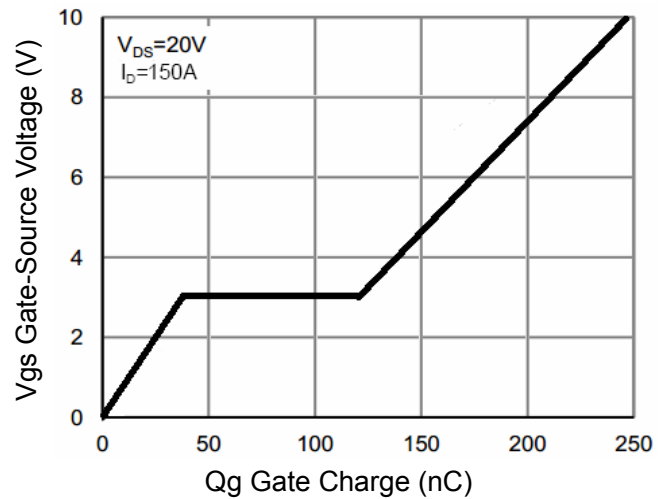


Figure 5 Gate Charge

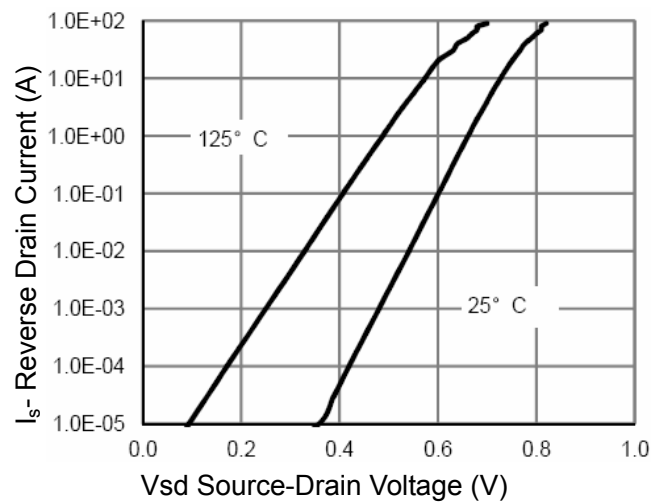


Figure 6 Source- Drain Diode Forward

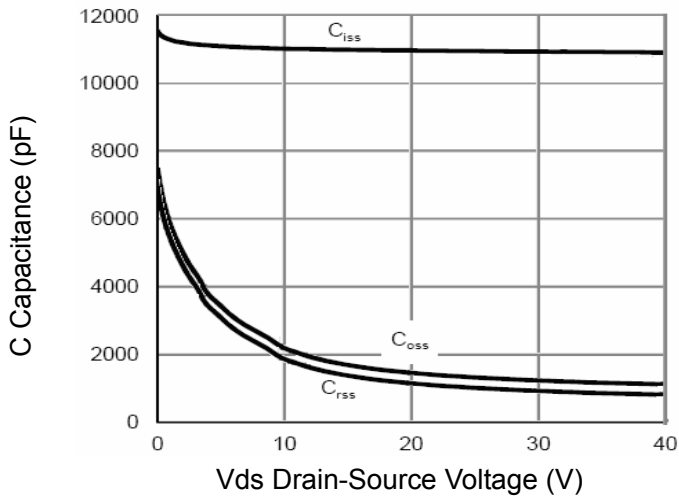


Figure 7 Capacitance vs Vds

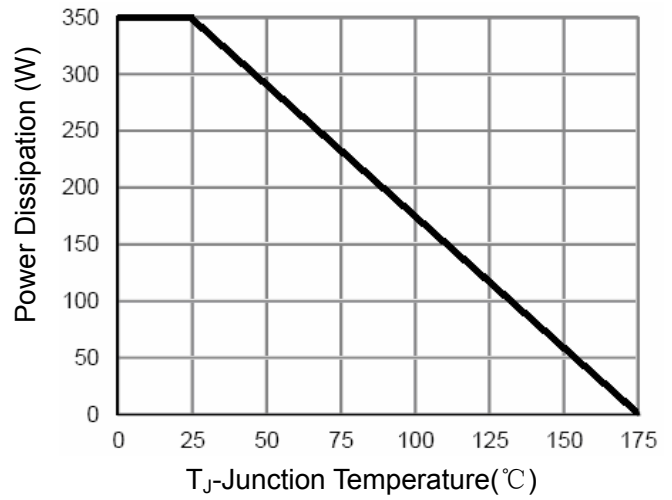


Figure 9 Power De-rating

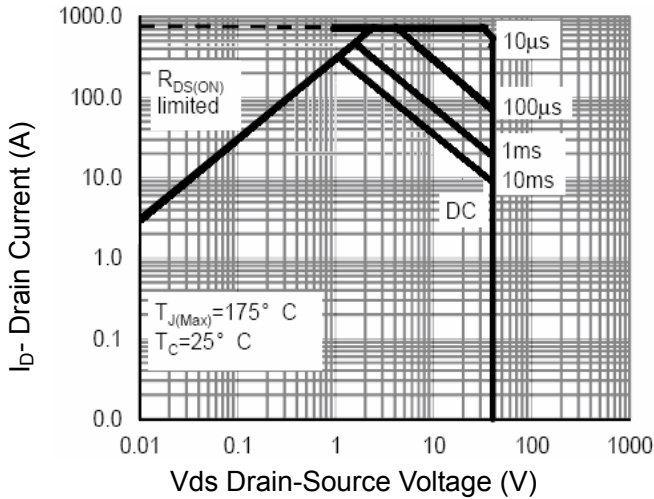


Figure 8 Safe Operation Area

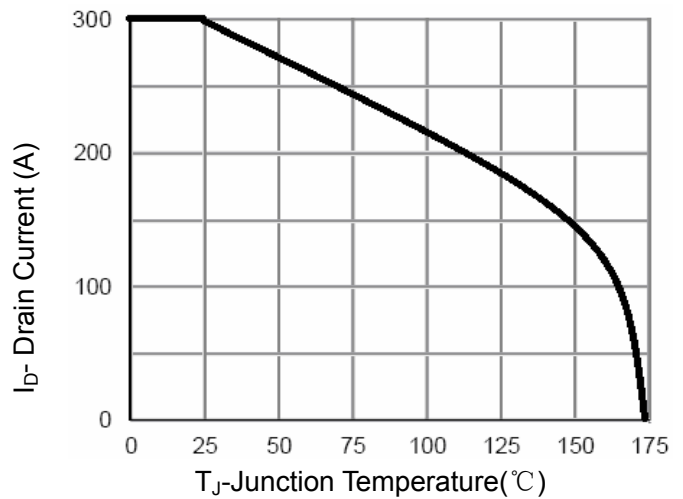


Figure 10 Current De-rating

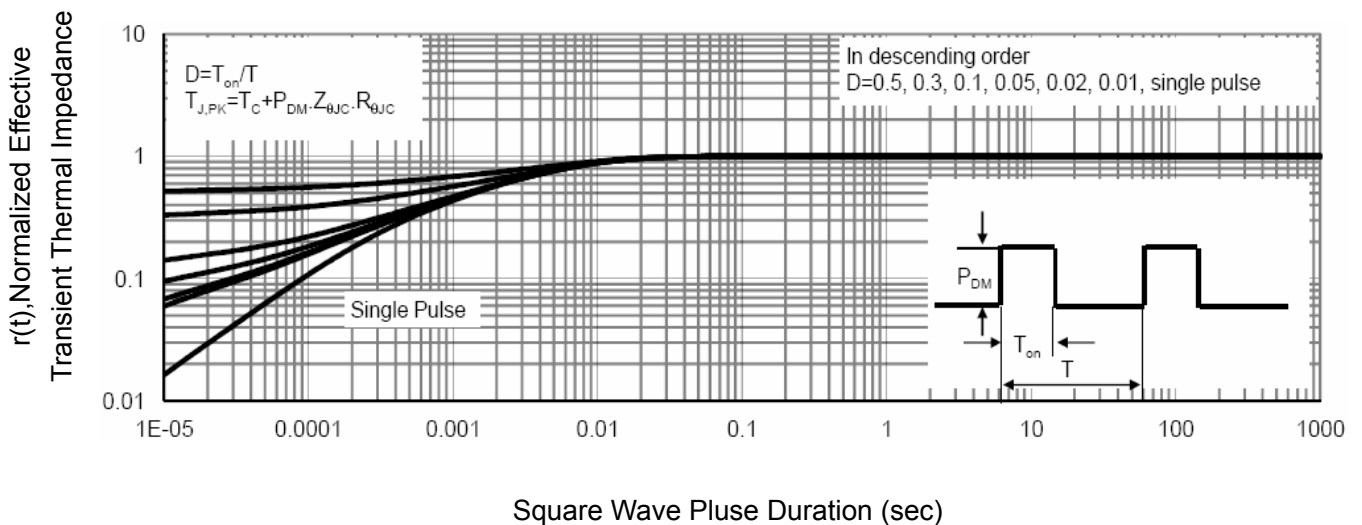
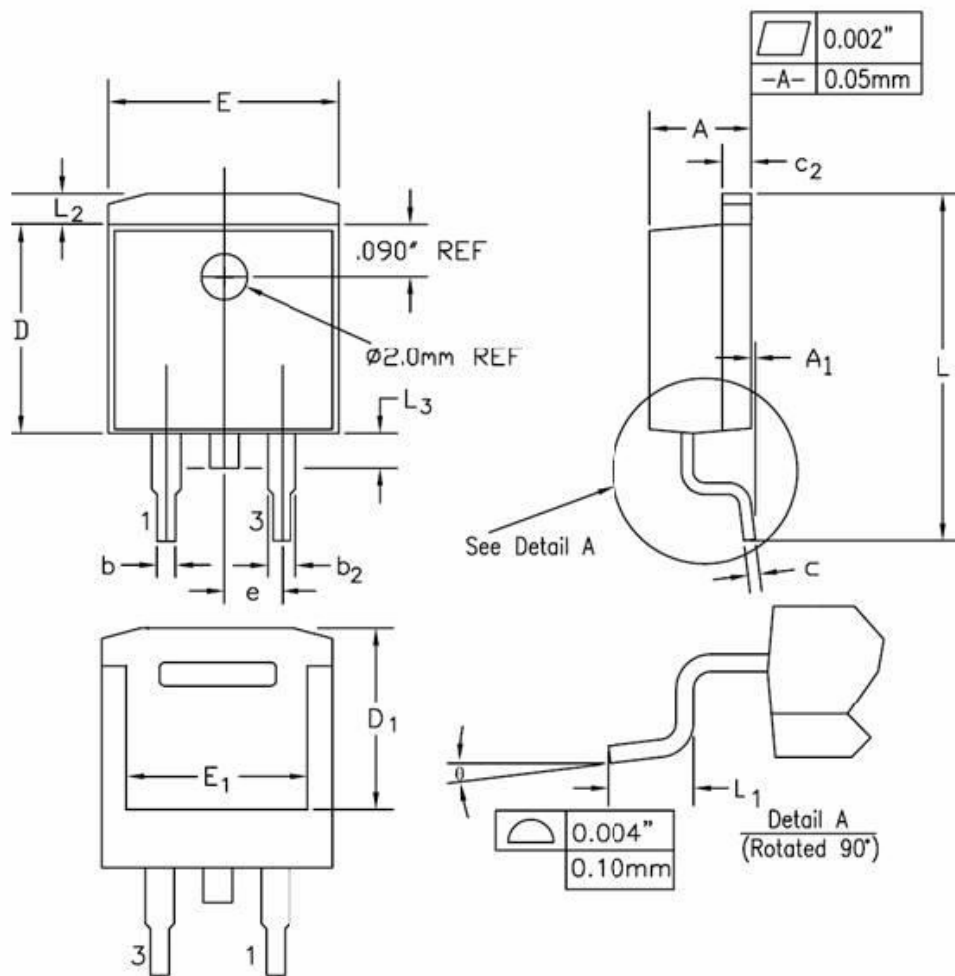


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	
A1	-	0.010	-	0.25	
b	0.028	0.037	0.71	0.94	
b2	0.045	0.055	1.15	1.40	
c	0.018	0.024	0.46	0.61	
c2	0.048	0.055	1.22	1.40	
D	0.350	0.370	8.89	9.40	
D1	0.315	0.324	8.01	8.23	
E	0.395	0.405	10.04	10.28	
E1	0.310	0.318	7.88	8.08	
e	0.100 BSC.		2.54 BSC.		
L	0.580	0.620	14.73	15.75	
L1	0.090	0.110	2.29	2.79	
L2	0.045	0.055	1.15	1.39	
L3	0.050	0.070	1.27	1.77	
θ	0°	8°	0°	8°	

Attention

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