

NCE N-Channel Enhancement Mode Power MOSFET

Description

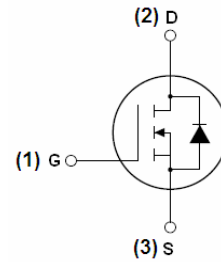
The VCRR2030K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

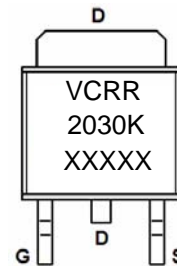
- $V_{DS} = 20V, I_D = 30A$
- $R_{DS(ON)} < 12m\Omega @ V_{GS} = 10V$ (Typ: 10.5m Ω)
- $R_{DS(ON)} < 13m\Omega @ V_{GS} = 4.5V$ (Typ: 11m Ω)
- $R_{DS(ON)} < 18m\Omega @ V_{GS} = 2.5V$ (Typ: 14m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

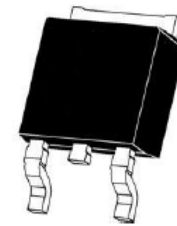
- Power switching application
- Load switching
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR2030K		TO-252-2L

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	21	A
Pulsed Drain Current	I_{DM}	100	A
Maximum Power Dissipation	P_D	40	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.8	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

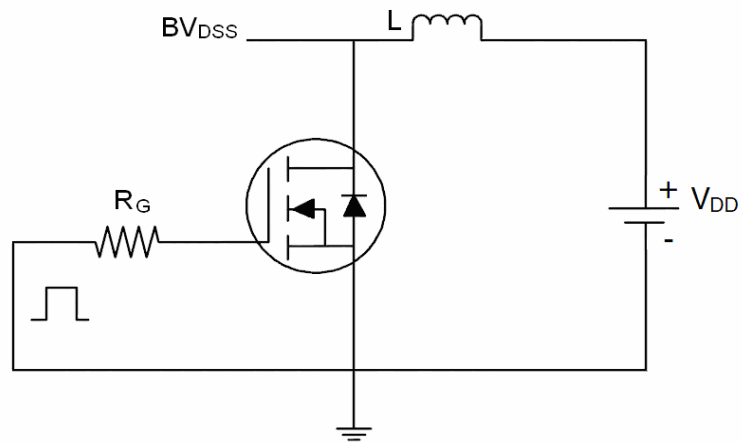
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	10.5	12	$m\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	11	13	$m\Omega$
		$V_{GS}=2.5V, I_D=20A$	-	14	18	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$		1544		PF
Output Capacitance	C_{oss}			210.1		PF
Reverse Transfer Capacitance	C_{rss}			201.4		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{GS}=10V, V_{DS}=10V$ $R_L=0.5\Omega, R_{GEN}=3\Omega$	-	4.5	-	nS
Turn-on Rise Time	t_r		-	9.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	18.7	-	nS
Turn-Off Fall Time	t_f		-	3.3	-	nS
Total Gate Charge	Q_g	$V_{GS}=4.5V, V_{DS}=10V, I_D=20A$		23.5		nC
Gate-Source Charge	Q_{gs}			2.8		nC
Gate-Drain Charge	Q_{gd}			5.75		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	30	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ (Note 3)	-	18	-	nS
Reverse Recovery Charge	Q_{rr}		-	9.5	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

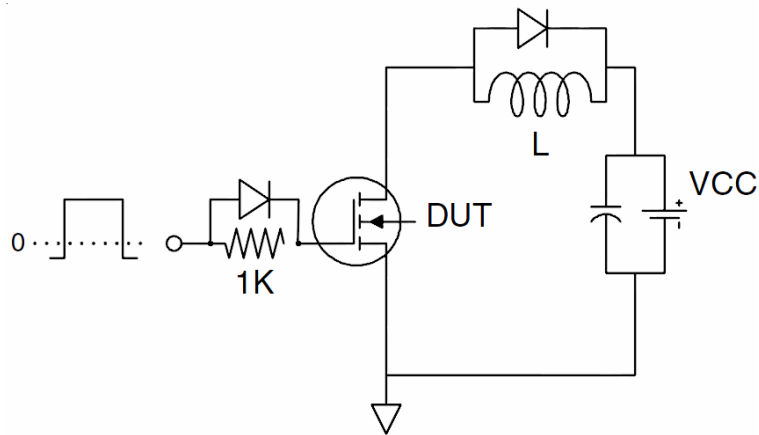
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=10V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

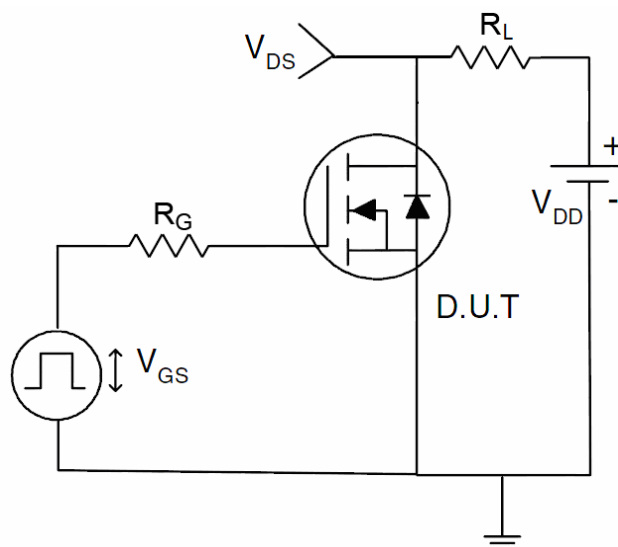
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

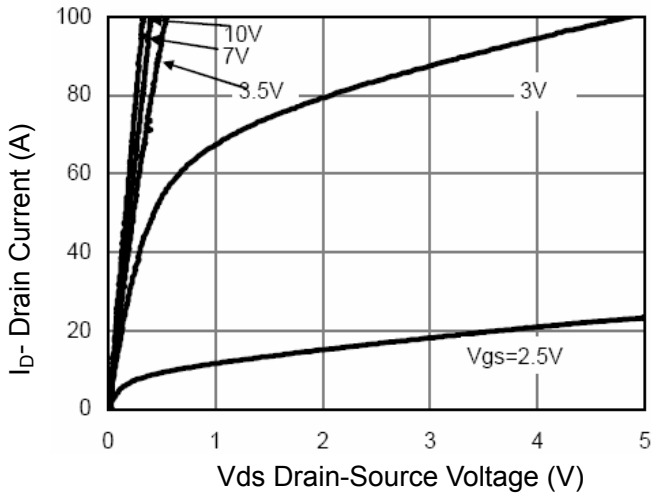


Figure 1 Output Characteristics

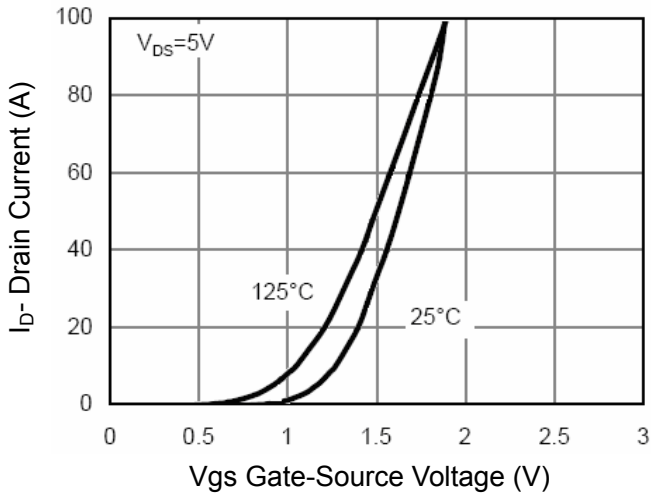


Figure 2 Transfer Characteristics

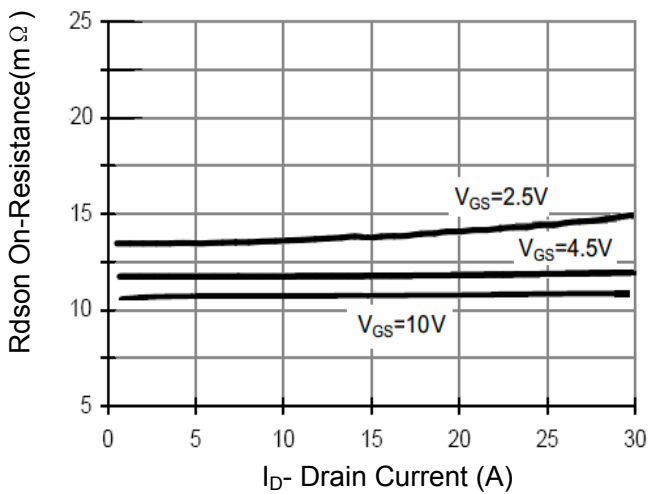


Figure 3 Rdson- Drain Current

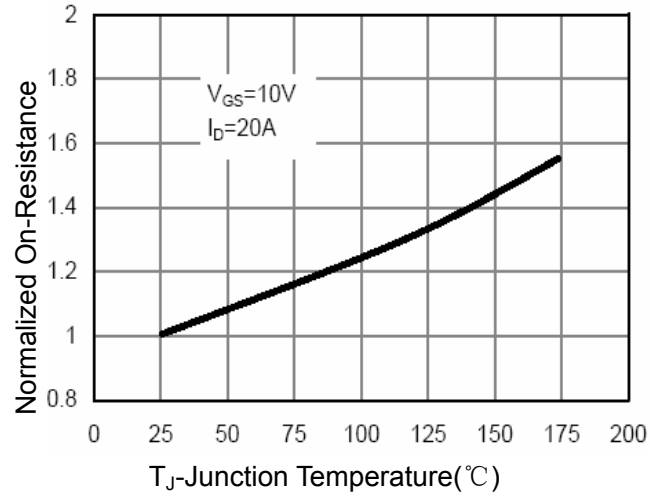


Figure 4 Rdson-Junction Temperature

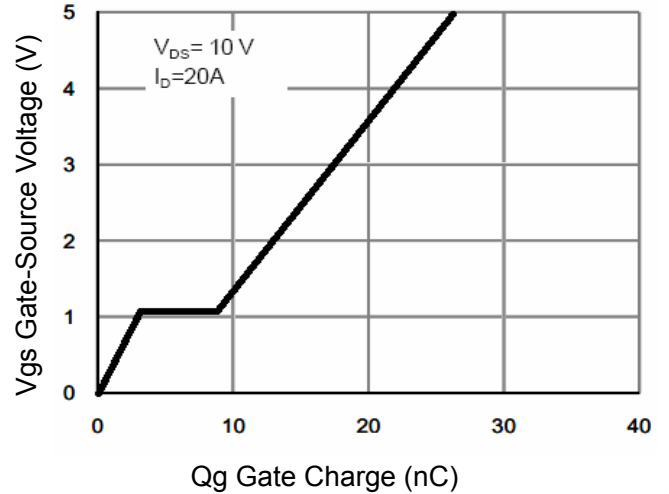


Figure 5 Gate Charge

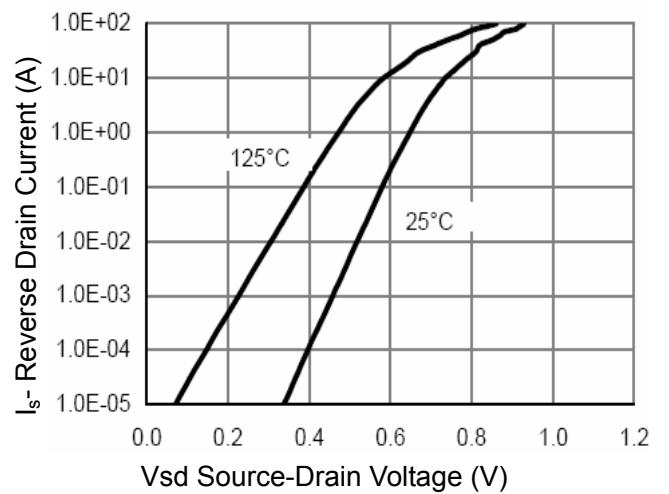


Figure 6 Source- Drain Diode Forward

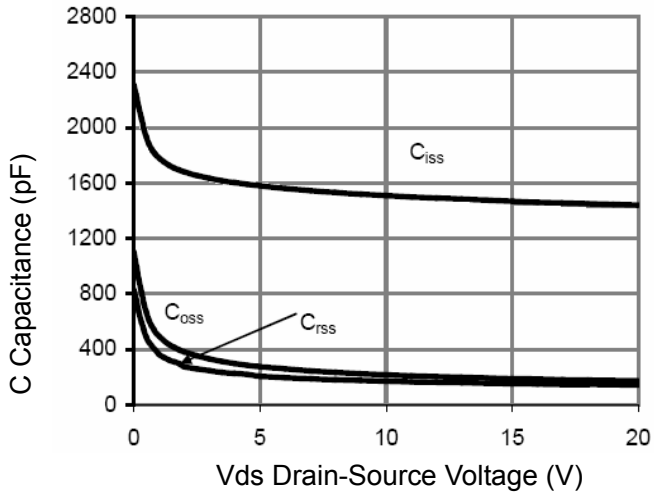


Figure 7 Capacitance vs Vds

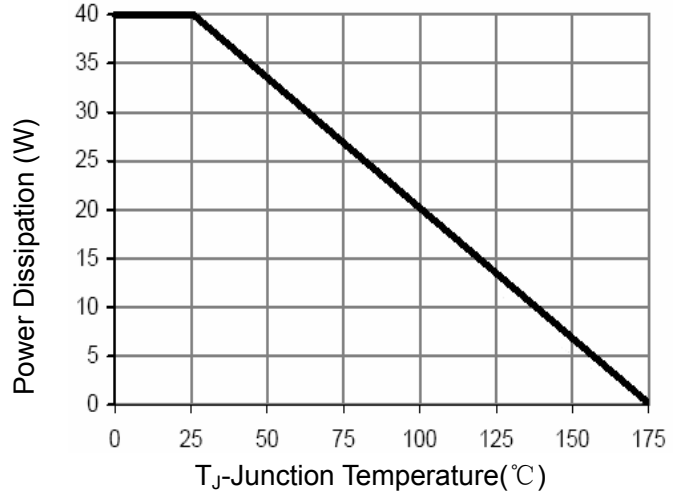


Figure 9 Power De-rating

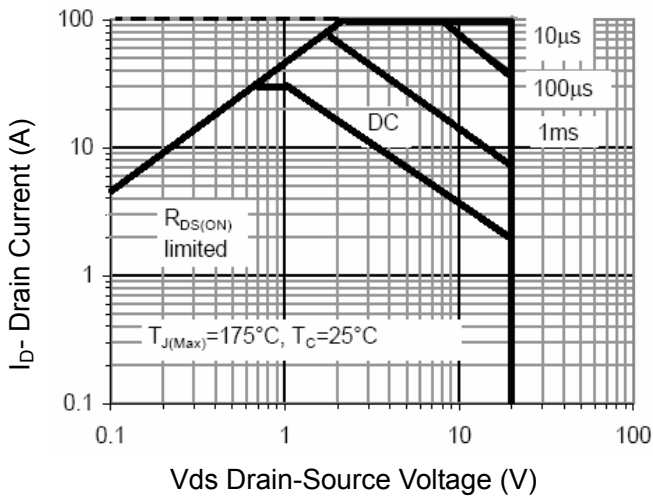


Figure 8 Safe Operation Area

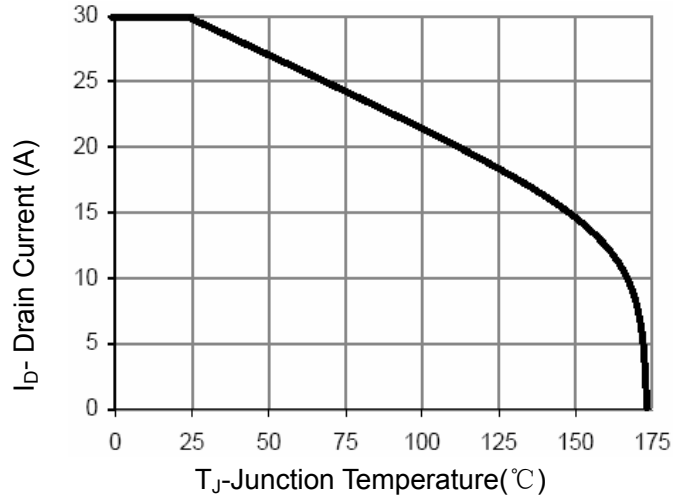


Figure 10 Current De-rating

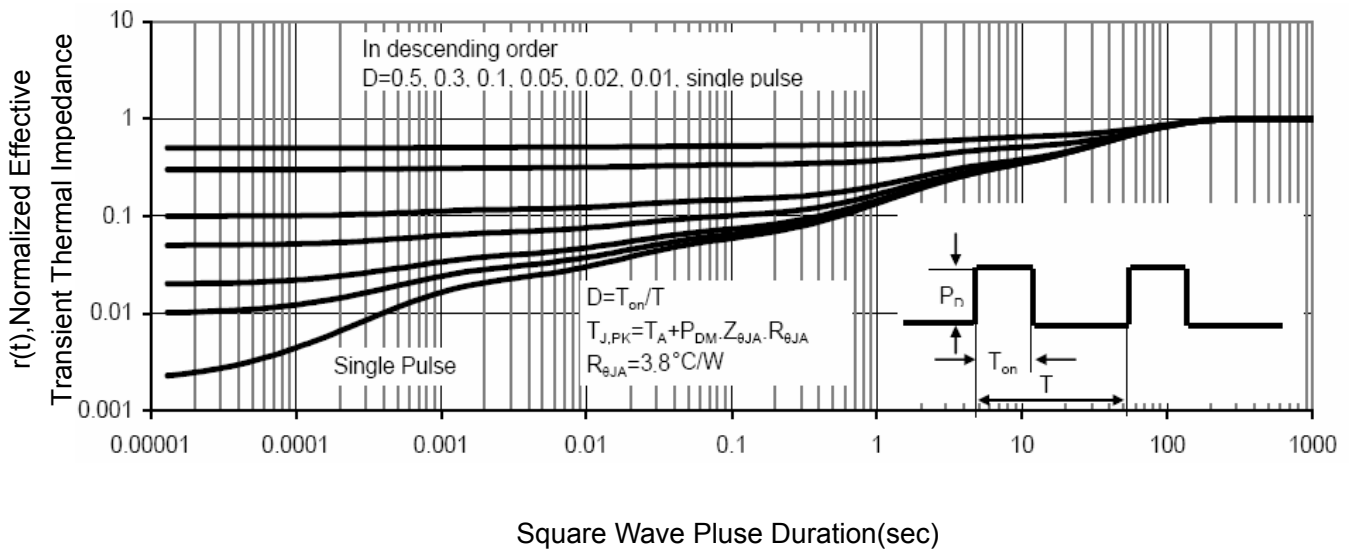
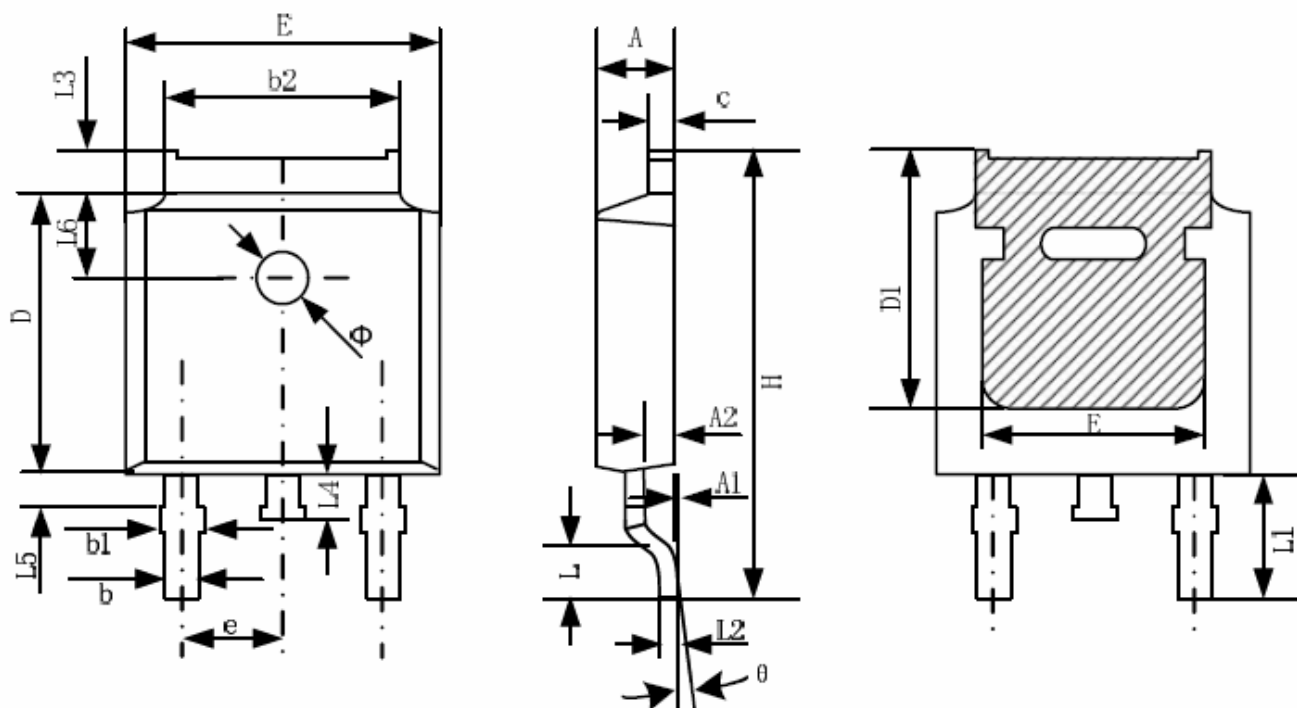


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°

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