

QIAOXIN N-Channel Enhancement Mode Power MOSFET

Description

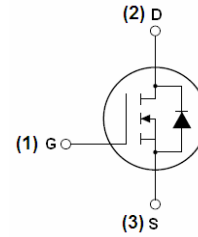
The VCRR0130KA uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

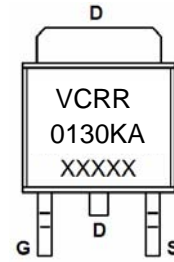
- $V_{DS} = 100V, I_D = 30A$
 $R_{DS(ON)} < 32m\Omega @ V_{GS}=10V$ (Typ:25m Ω)
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=4.5V$ (Typ:28m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

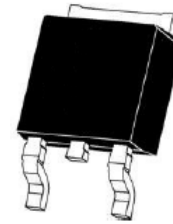
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR0130KA		TO-252-2L

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	21	A
Pulsed Drain Current ^(Note 1)	I_{DM}	120	A
Maximum Power Dissipation	P_D	85	W
Derating factor		0.57	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	200	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
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Electrical Characteristics (T_C=25°C unless otherwise noted)

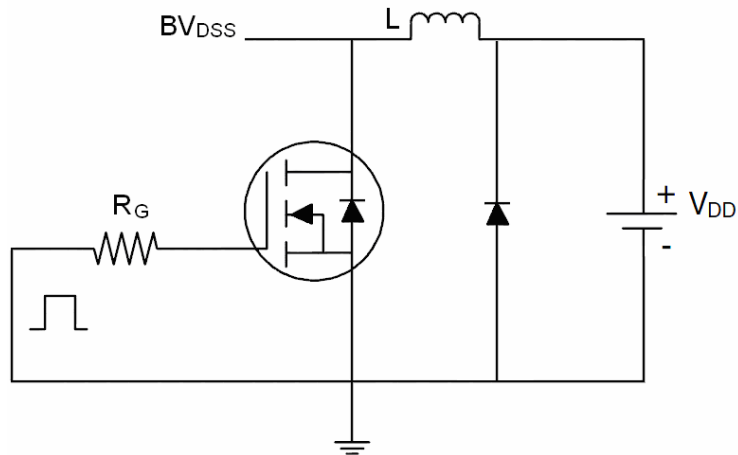
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
B _V DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	115	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.9	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =10A	-	25	32	mΩ
		V _{GS} =4.5V, I _D =10A	-	28	35	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A	-	15	-	S
Dynamic Characteristics (Note 4)						
C _{ISS}	Input Capacitance	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	2479	-	PF
C _{OSS}	Output Capacitance		-	96	-	PF
C _{RSS}	Reverse Transfer Capacitance		-	79	-	PF
Switching Characteristics (Note 4)						
t _{d(on)}	Turn-on Delay Time	V _{DD} =50V, R _L =5Ω V _{GS} =10V, R _{GEN} =3Ω	-	9	-	nS
t _r	Turn-on Rise Time		-	9	-	nS
t _{d(off)}	Turn-Off Delay Time		-	32	-	nS
t _f	Turn-Off Fall Time		-	8	-	nS
Q _g	Total Gate Charge	V _{DS} =50V, I _D =10A, V _{GS} =10V	-	67.2	-	nC
Q _{gs}	Gate-Source Charge		-	9.4	-	nC
Q _{gd}	Gate-Drain Charge		-	15.5	-	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage (Note 3)	V _{GS} =0V, I _S =10A	-	-	1.2	V
I _S	Diode Forward Current (Note 2)	-	-	-	30	A
t _{rr}	Reverse Recovery Time	T _J = 25°C, I _F = 10A	-	32	-	nS
Q _{rr}	Reverse Recovery Charge	di/dt = 100A/μs (Note 3)	-	53	-	nC
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

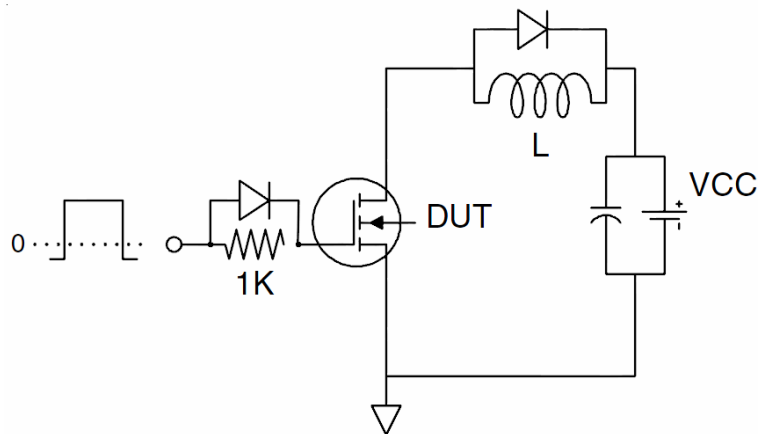
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS Condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω

Test Circuit

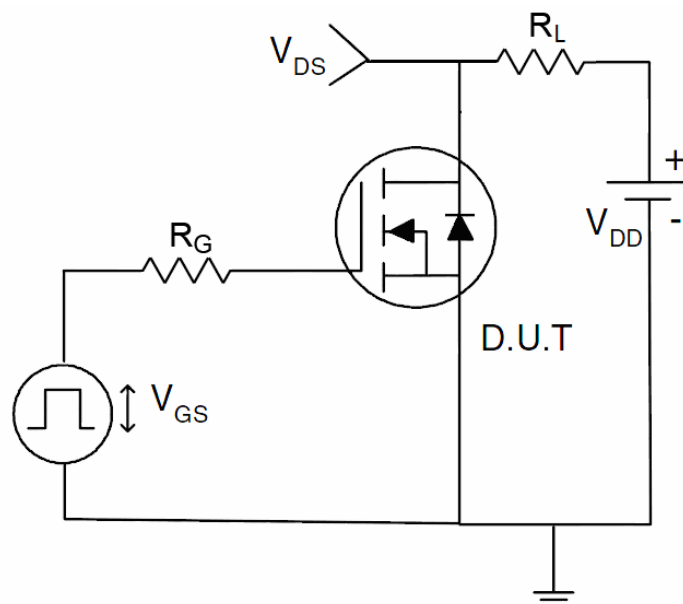
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

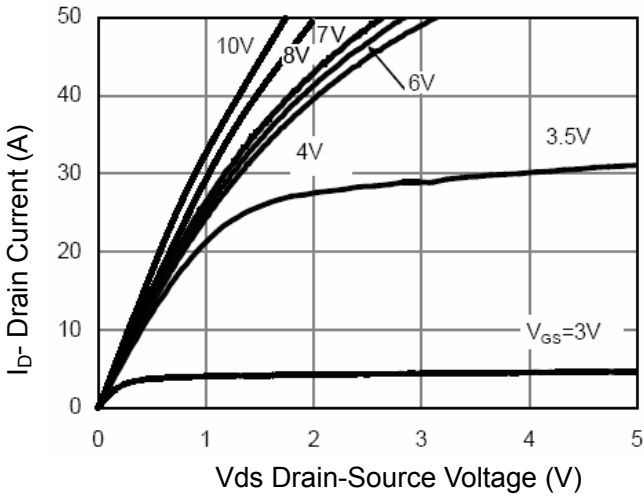


Figure 1 Output Characteristics

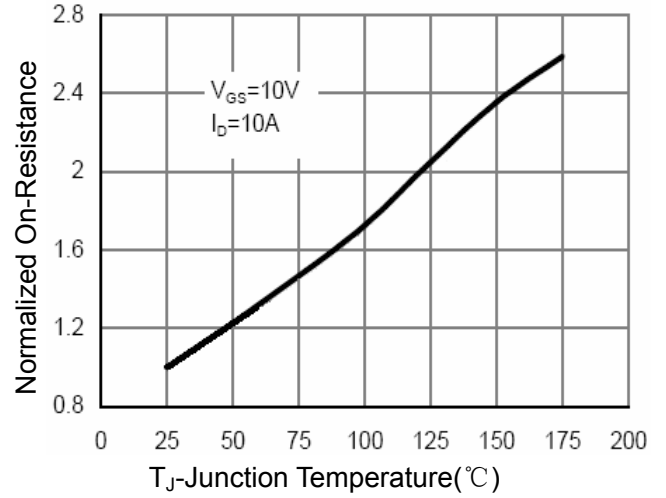


Figure 4 Rdson-Junction Temperature

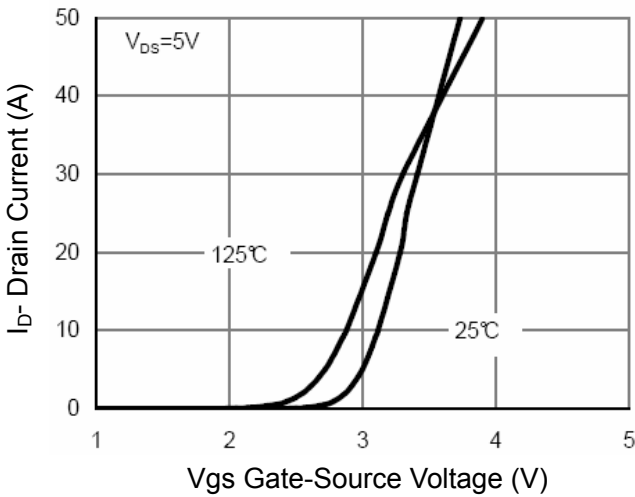


Figure 2 Transfer Characteristics

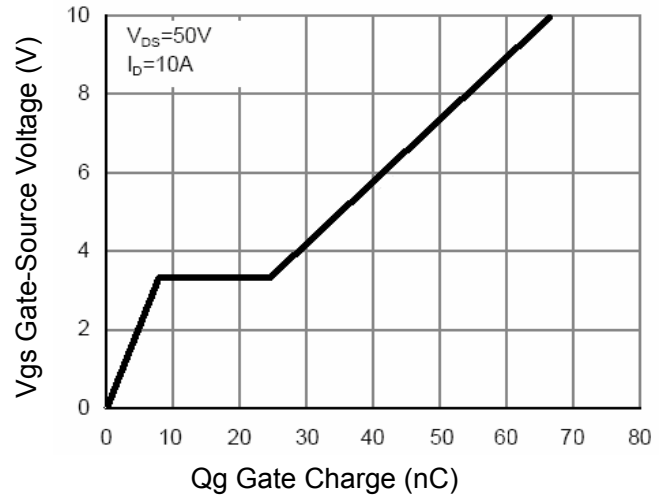


Figure 5 Gate Charge

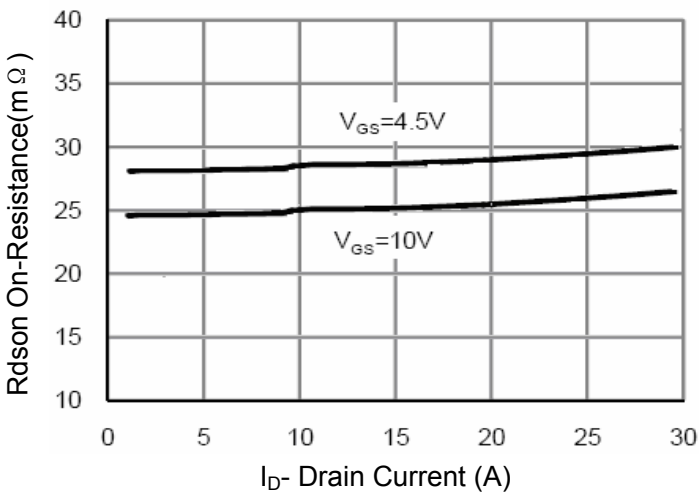


Figure 3 Rdson- Drain Current

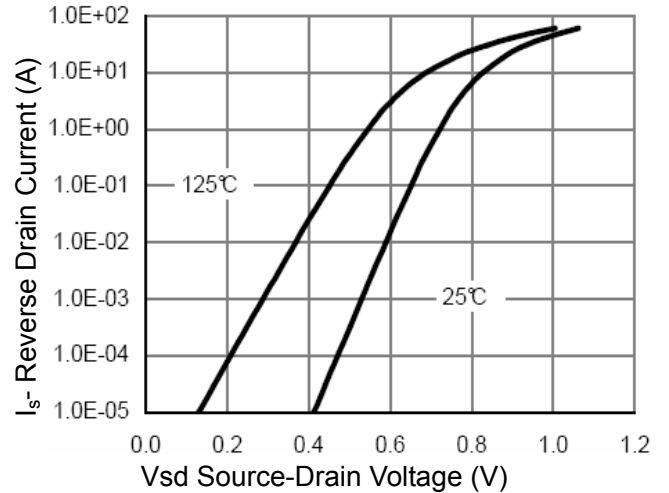


Figure 6 Source- Drain Diode Forward

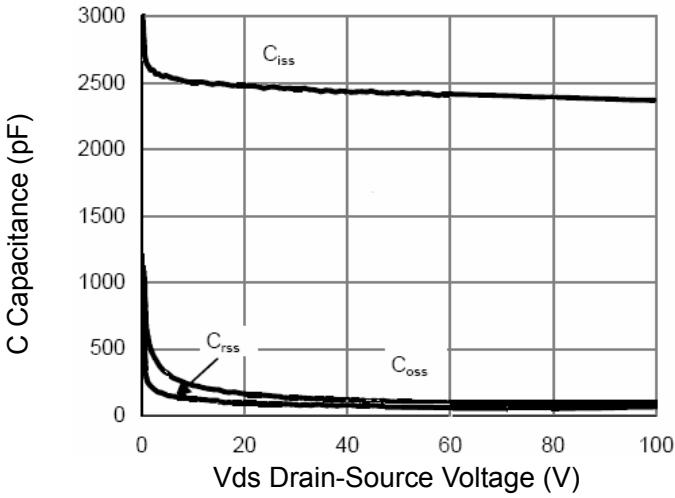


Figure 7 Capacitance vs Vds

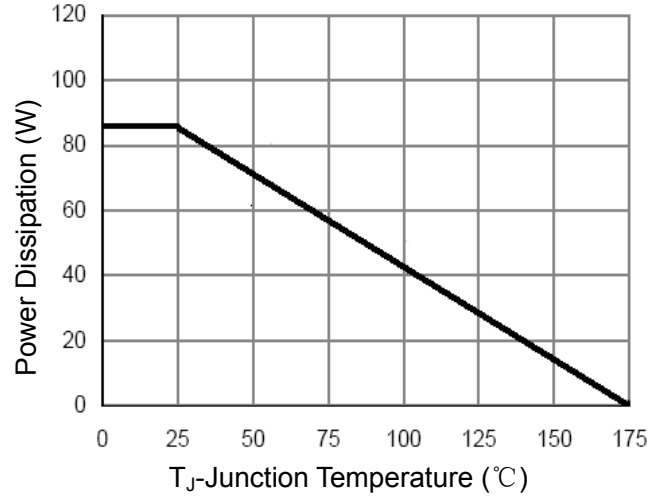


Figure 9 Power De-rating

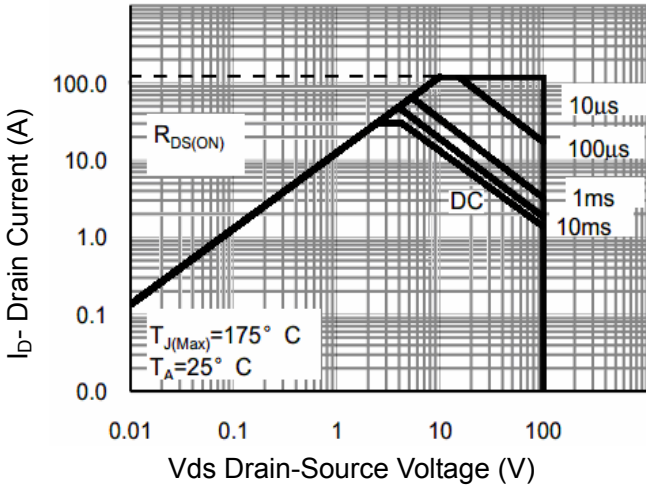


Figure 8 Safe Operation Area

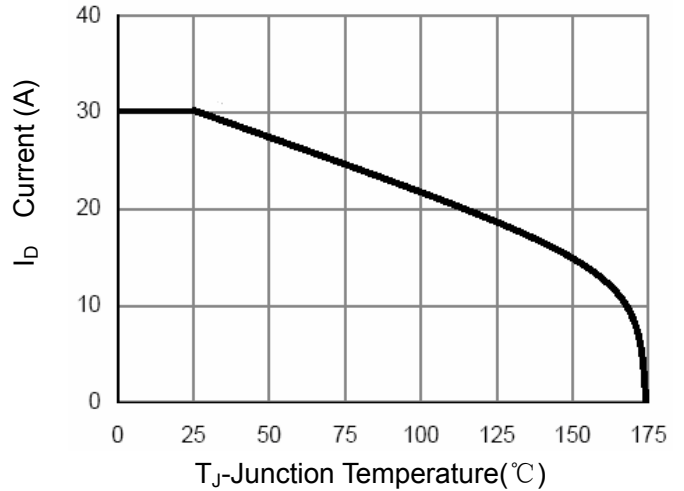


Figure 10 ID Current- Junction Temperature

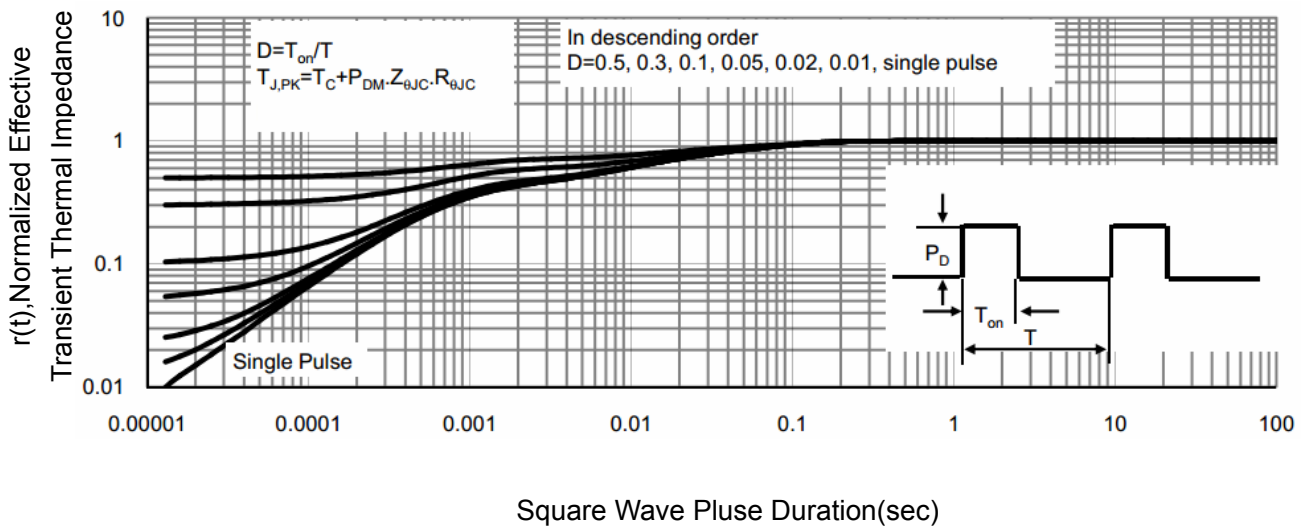
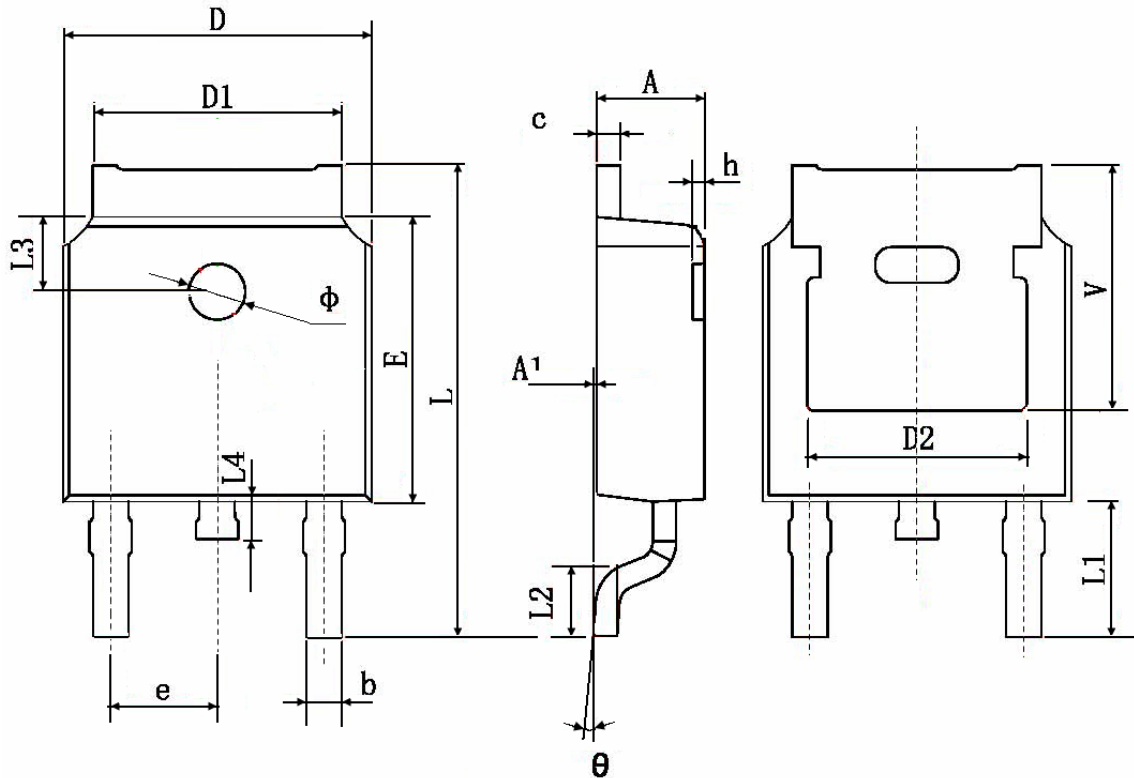


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
phi	1.100	1.300	0.043	0.051
theta	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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