

QIAOXIN N-Channel Enhancement Mode Power MOSFET

Description

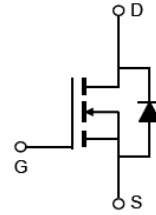
The VCRR1507AK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

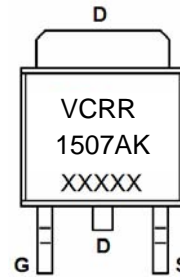
- $V_{DS} = 150V, I_D = 7A$
 $R_{DS(ON)} < 300m\Omega @ V_{GS}=10V$ (Typ:280m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

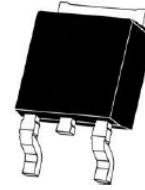
- Power switching application
- Hard switched and high frequency circuits



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VCRR1507AK	VCRR1507AK	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	7	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	4.3	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	28	A
Maximum Power Dissipation	P_D	30	W
Avalanche Current ^(Note 1)	I_{AR}	4.5	A
Single pulse avalanche energy ^(Note 5)	E_{AS}	6	mJ
Drain Source voltage slope, $V_{DS} \leq 120\text{ V}$,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 120\text{ V}$, $I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	5	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

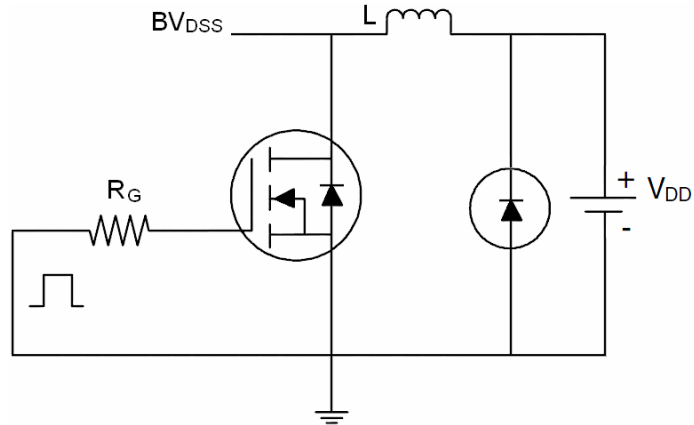
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3A$	-	235	255	m Ω
		$V_{GS}=10V, I_D=7A$	-	280	300	m Ω
Gate resistance	R_G		-	1.7	-	Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=7A$	-	3	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=75V, V_{GS}=0V,$ $F=1.0MHz$	-	544	-	PF
Output Capacitance	C_{oss}		-	13.8	-	PF
Reverse Transfer Capacitance	C_{rss}		-	10.5	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=75V, R_L=10\Omega$ $V_{GS}=10V, R_G=6\Omega$	-	8	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{DS}=75V, I_D=7A,$ $V_{GS}=10V$	-	20.3	-	nC
Gate-Source Charge	Q_{gs}		-	3.2	-	nC
Gate-Drain Charge	Q_{gd}		-	5.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=7A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	7	A

Notes:

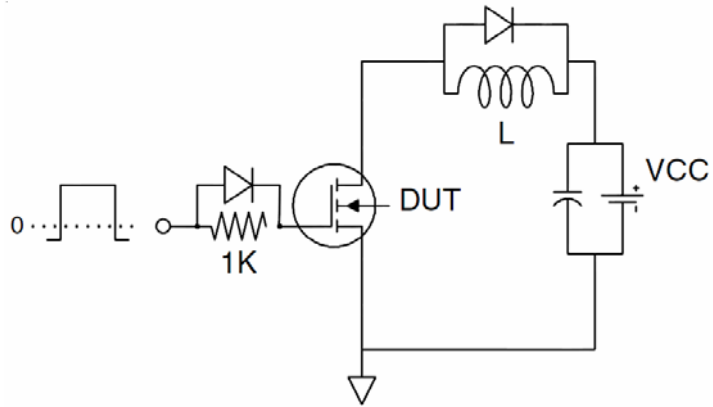
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to product
5. EAS condition : $T_j=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

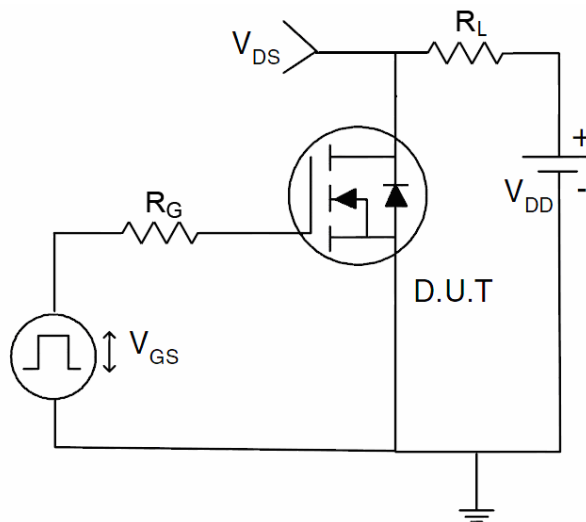
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

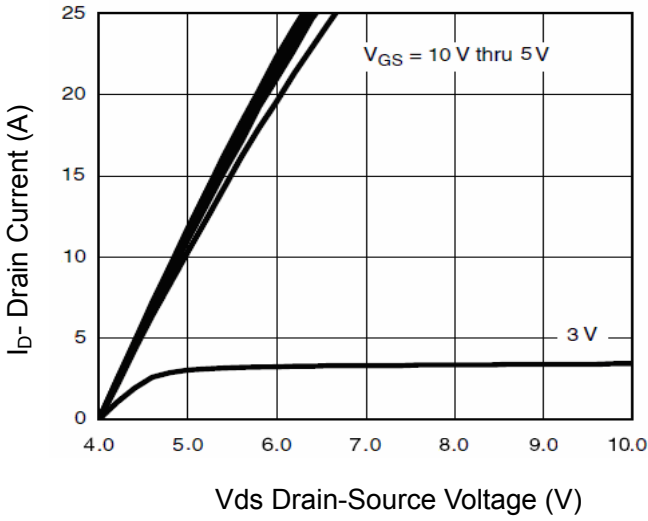


Figure 1 Output Characteristics

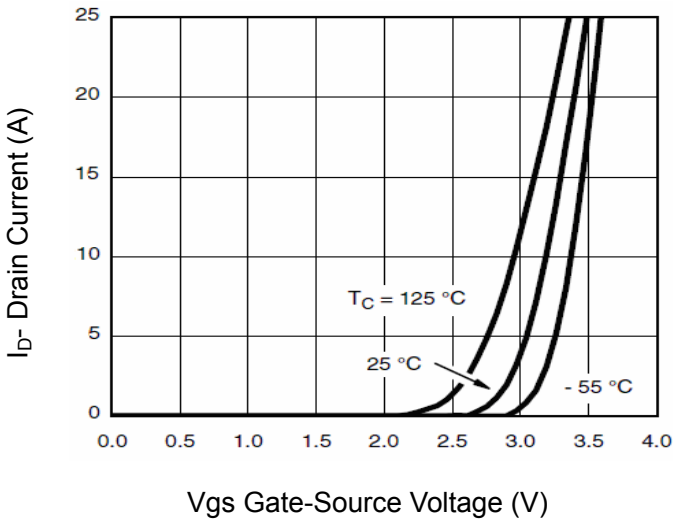


Figure 2 Transfer Characteristics

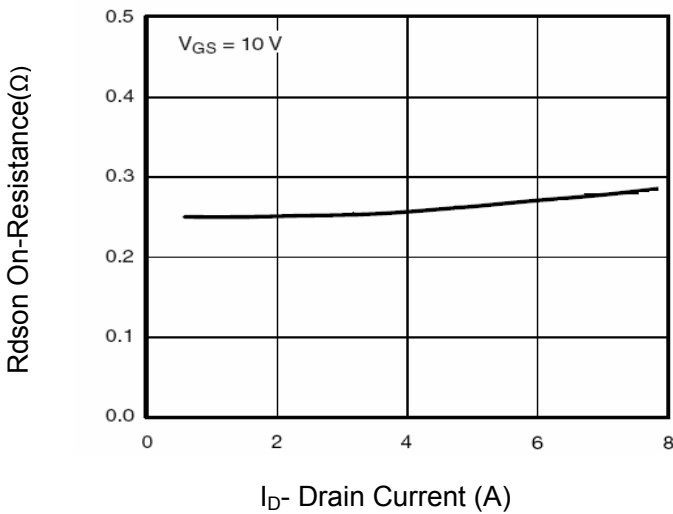


Figure 3 Rdson- Drain Current

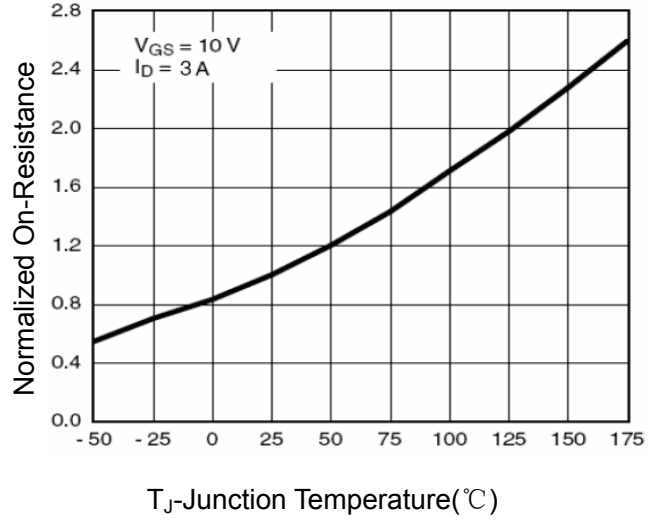


Figure 4 Rdson- Junction Temperature

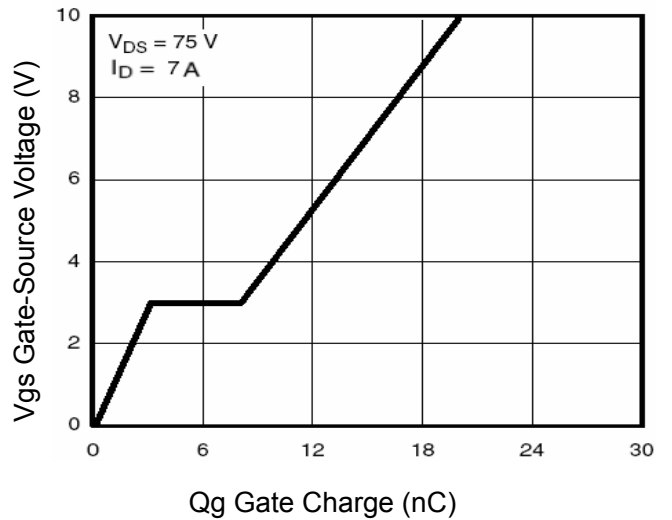


Figure 5 Gate Charge

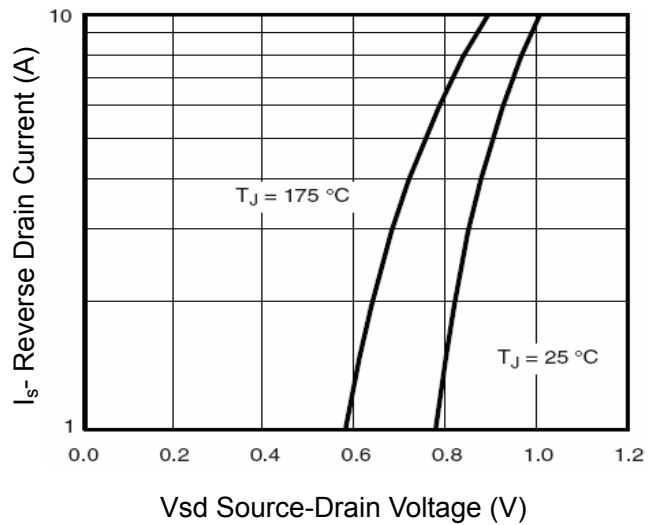
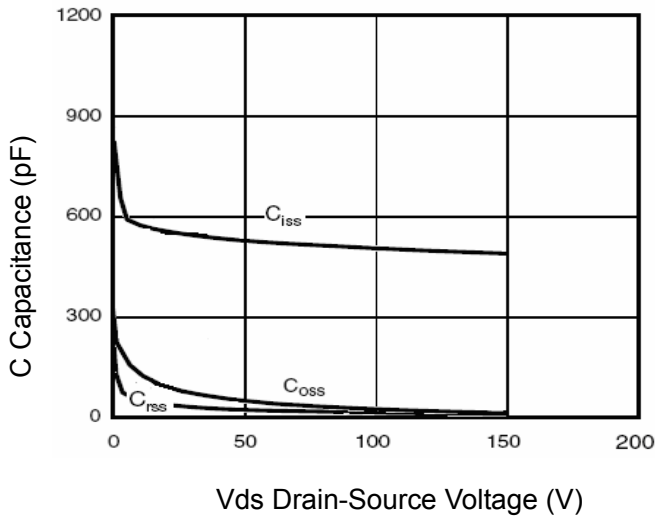
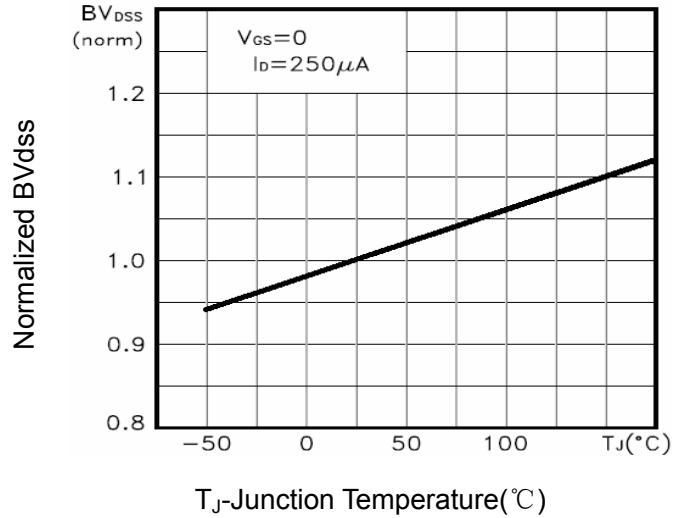


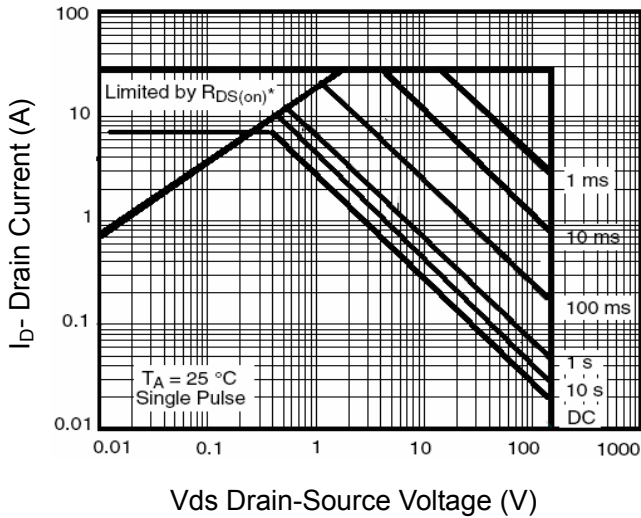
Figure 6 Source- Drain Diode Forward



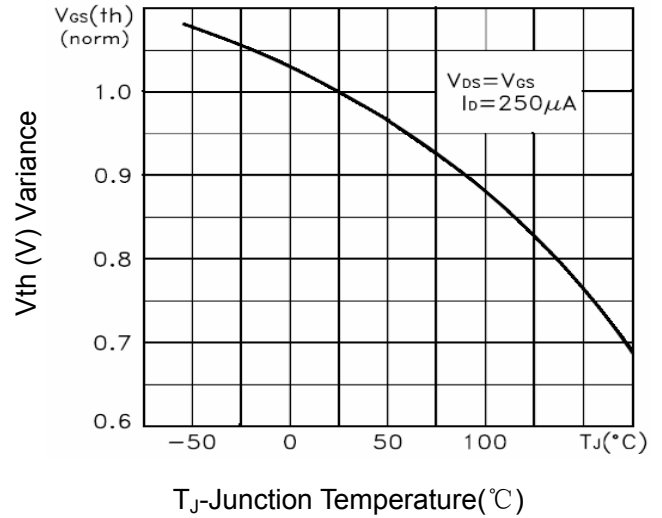
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

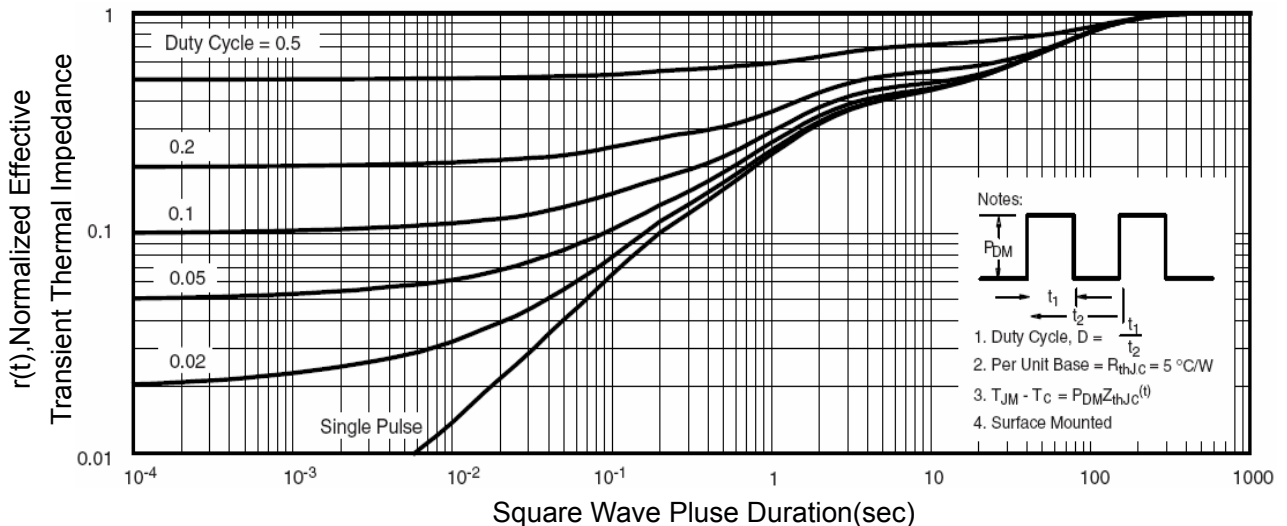
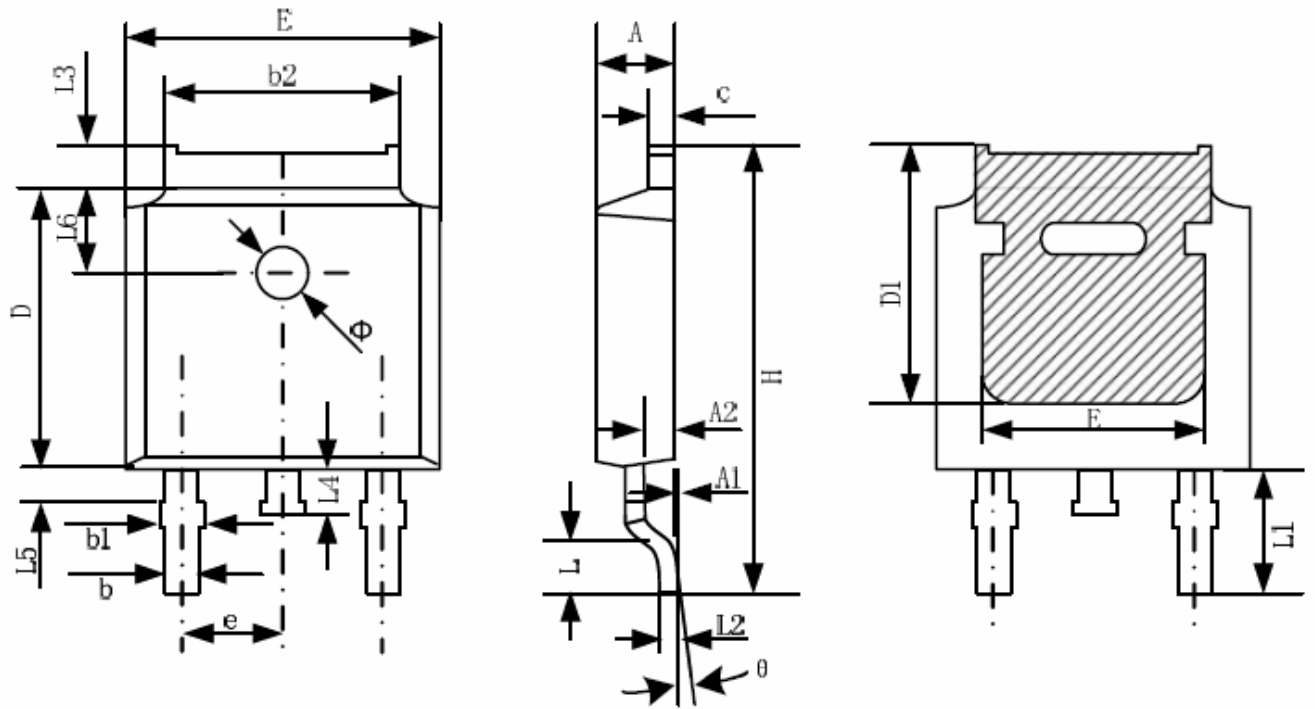


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°

Attention

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