

**QIAOXIN N-Channel Super Trench Power MOSFET**

**Description**

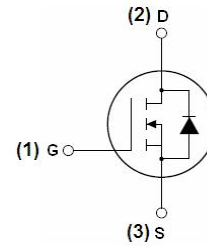
The VCRRP02T10T uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

**General Features**

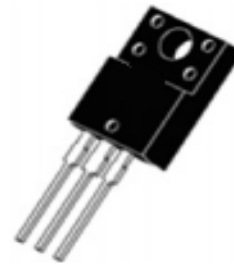
- $V_{DS} = 200V, I_D = 100A$   
 $R_{DS(ON)} < 12m\Omega @ V_{GS} = 10V$
- Excellent gate charge x  $R_{DS(on)}$  product
- Very low on-resistance  $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

**Application**

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic diagram



TO-247 top view

**Package Marking and Ordering Information**

Device Marking	Device	Device Package
VCRRP02T10T		TO-247-3L

**Absolute Maximum Ratings ( $T_c = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	100	A
Drain Current-Continuous( $T_c = 100^\circ C$ )	$I_D(100^\circ C)$	70.7	A
Pulsed Drain Current	$I_{DM}$	400	A
Maximum Power Dissipation	$P_D$	300	W
Derating factor		2	W/ $^\circ C$
Single pulse avalanche energy (Note 1)	$E_{AS}$	1216	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.5	$^\circ C/W$
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## Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

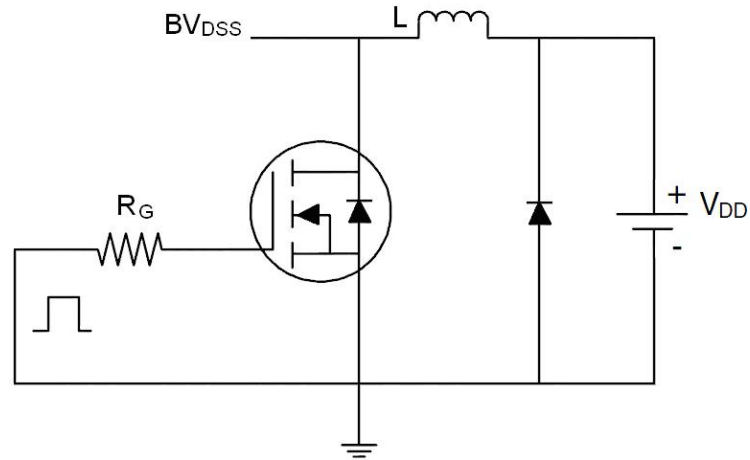
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	200		-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.5		4.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =50A	-	9.5	12	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =50A	70	-	-	S
<b>Dynamic Characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, F=1.0MHz	-	6000	-	PF
Output Capacitance	C <sub>oss</sub>		-	425	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	16	-	PF
<b>Switching Characteristics</b> (Note 2)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =100V, I <sub>D</sub> =50A V <sub>GS</sub> =10V, R <sub>G</sub> =4.7Ω	-	18	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	26	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	41	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	11	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =100V, I <sub>D</sub> =50A, V <sub>GS</sub> =10V	-	87		nC
Gate-Source Charge	Q <sub>gs</sub>		-	32		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	17.5		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =100A	-		1.2	V
Diode Forward Current	I <sub>S</sub>		-	-	100	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 50	-	140		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs	-	600		nC

### Notes:

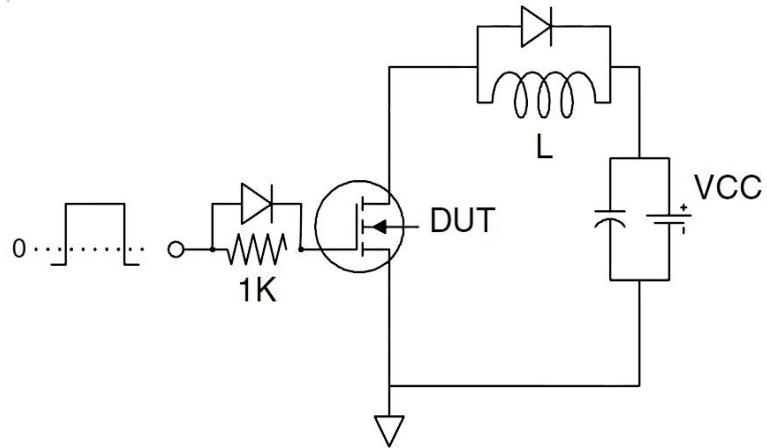
1. EAS condition : T<sub>j</sub>=25°C, V<sub>DD</sub>=50V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsin k, assuming a maximum junction temperature of T<sub>J</sub>(MAX)=175° C. The SOA curve provides a single pulse rating.

## Test Circuit

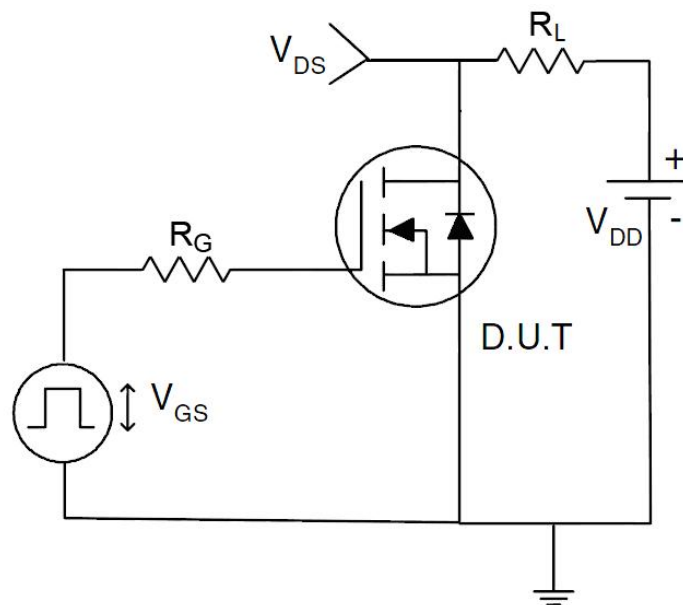
### 1) $E_{AS}$ test Circuit



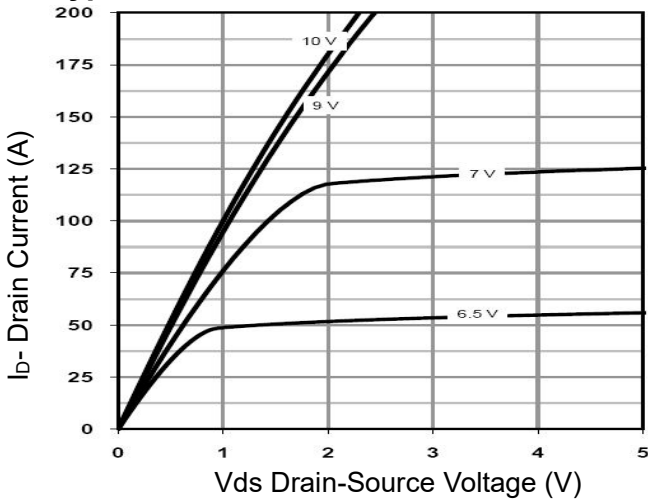
### 2) Gate charge test Circuit



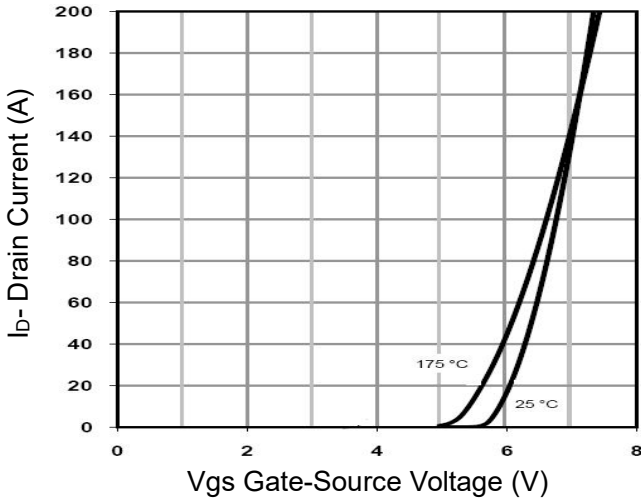
### 3) Switch Time Test Circuit



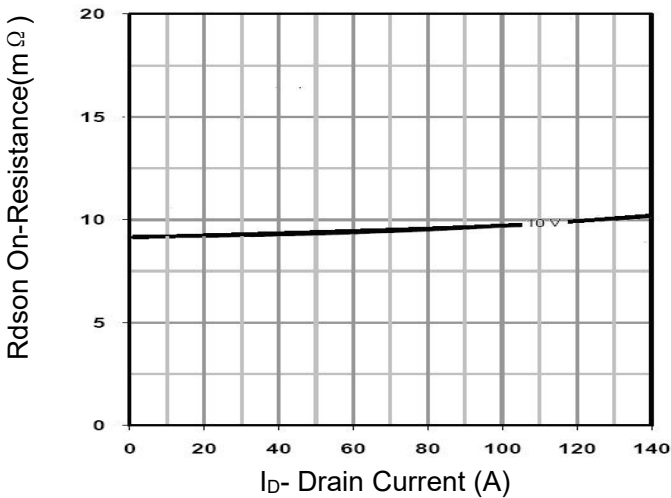
**Typical Electrical and Thermal Characteristics**



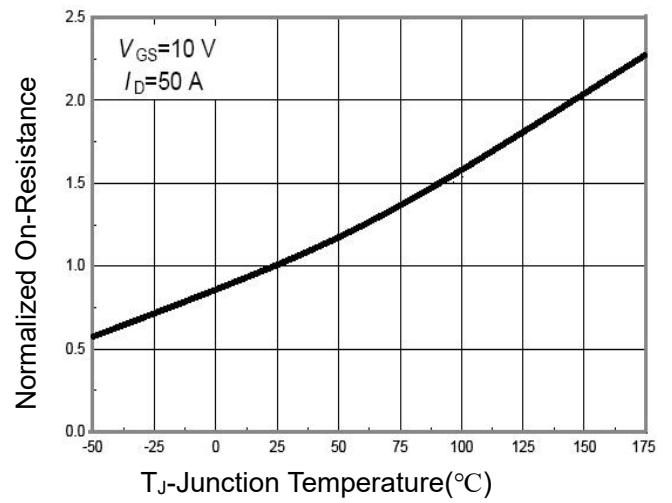
**Figure 1 Output Characteristics**



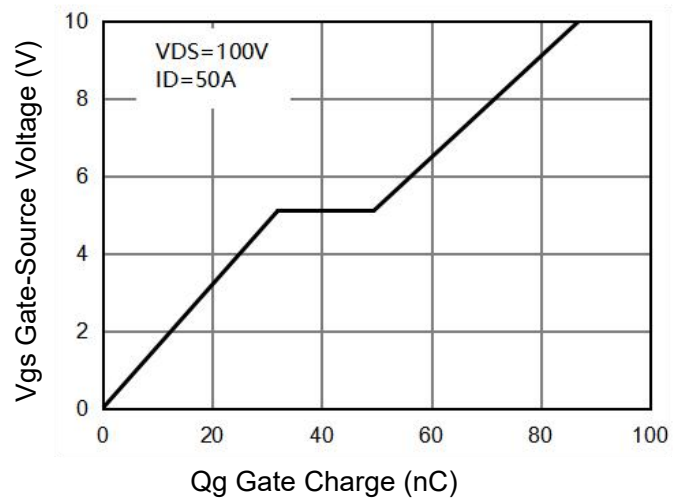
**Figure 2 Transfer Characteristics**



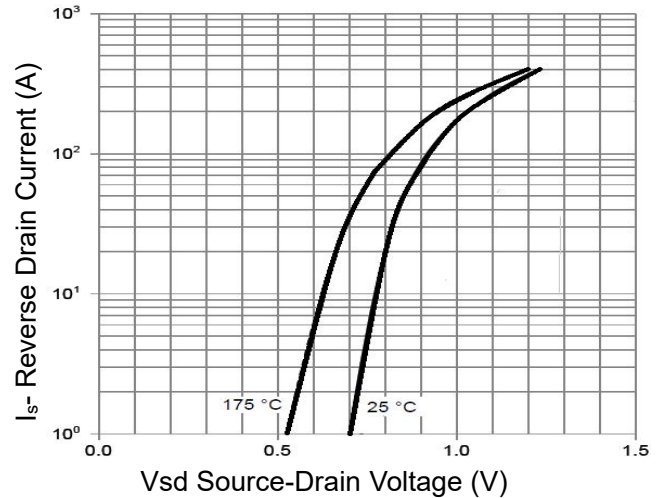
**Figure 3  $R_{DS(on)}$ - Drain Current**



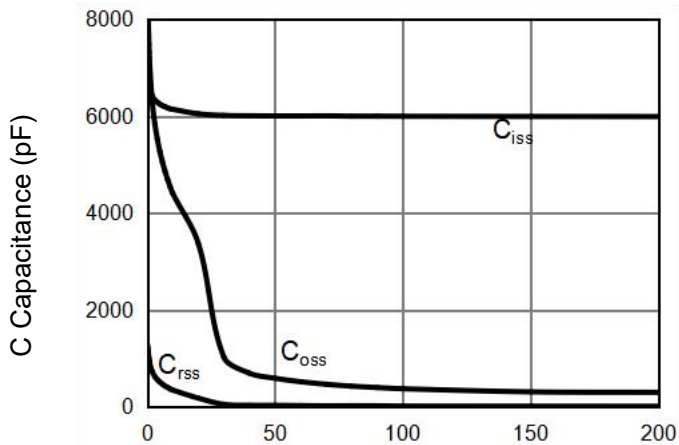
**Figure 4  $R_{DS(on)}$ -Junction Temperature**



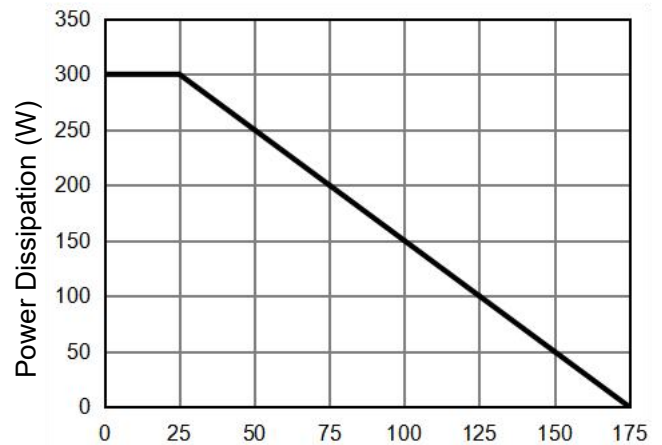
**Figure 5 Gate Charge**



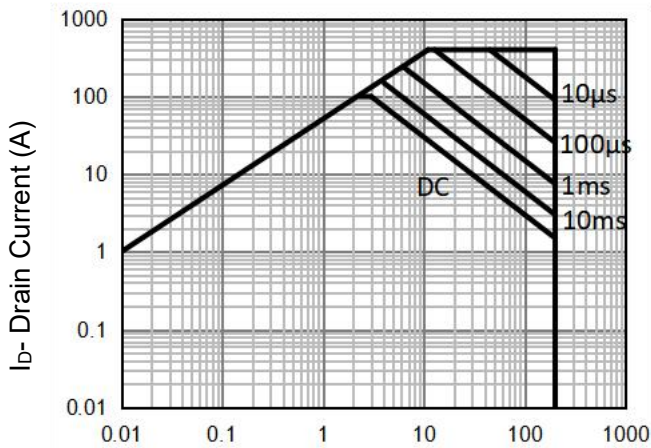
**Figure 6 Source- Drain Diode Forward**



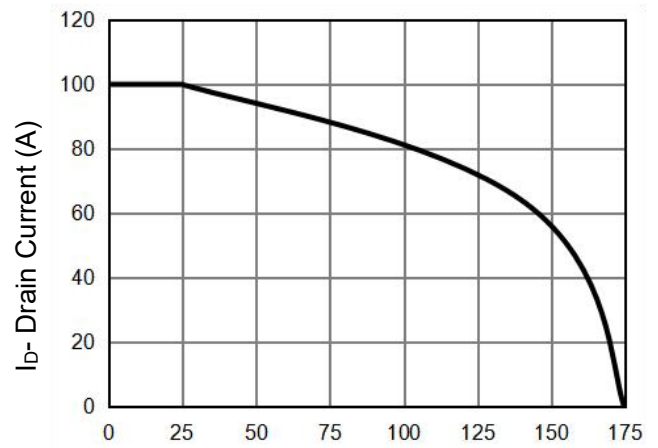
**Figure 7 Capacitance vs Vds**



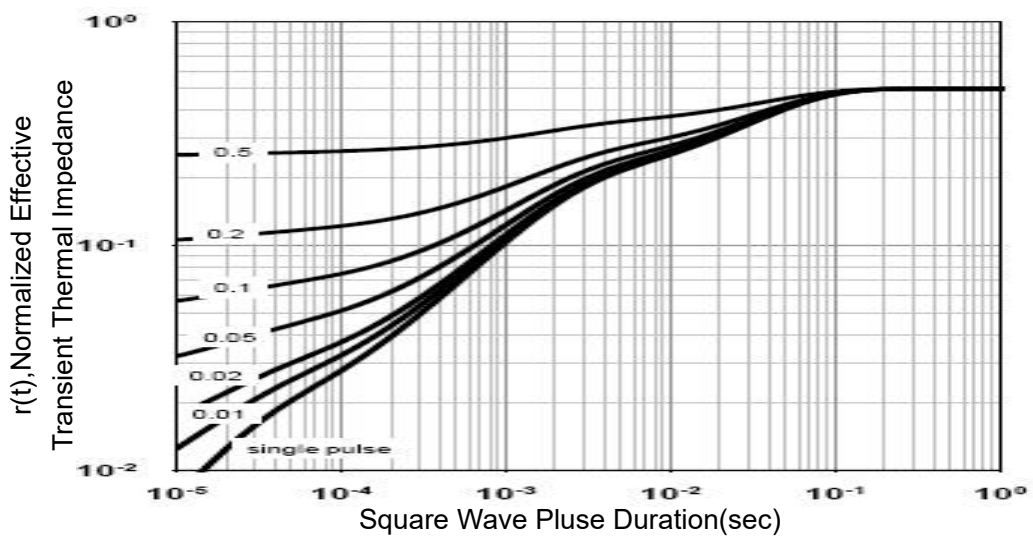
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

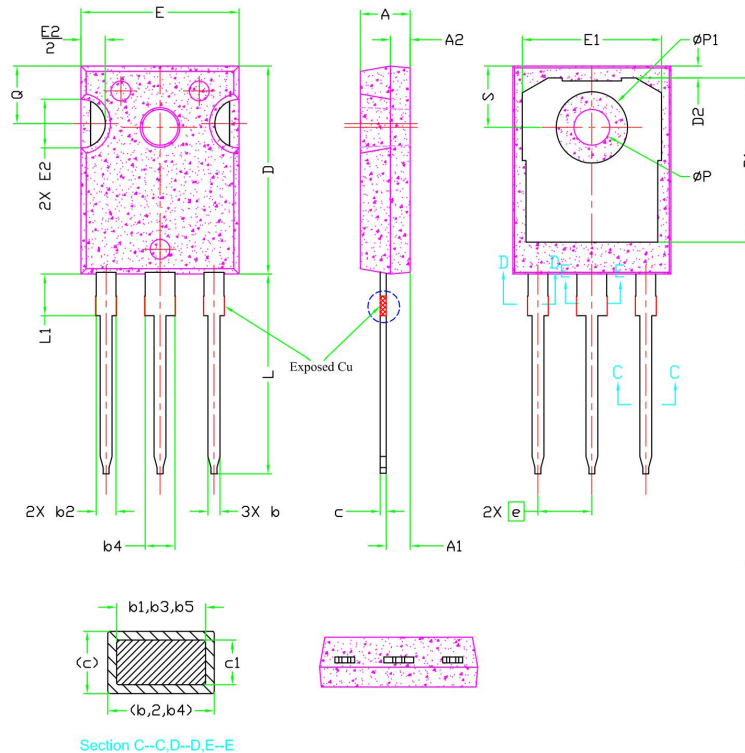


**Figure 10 Current De-rating**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## TO-247 Package Information



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
$\phi P$	3.56	3.61	3.65	7
$\phi P1$	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

Note:

1. Package Reference: JEDEC TO247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.
7.  $\phi P$  To Have A Maximum Draft Angle Of 1.5° To The Top Of The Part With A Maximum Hole Diameter Of 3.91mm.
8. Dimension "b2" And "b4" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.10mm Total In Excess Of "b2" And "b4" Dimension At Maximum Material Condition.

### Attention

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