QIAOXIN N-Channel Super Trench Power MOSFET

Description

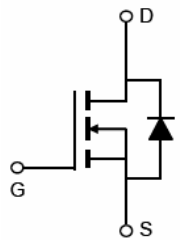
The VCRRP1520K uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

General Features

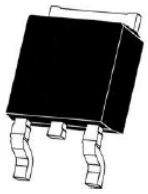
- V_{DS} =150V,I_D =20A
  $R_{DS(ON)}$=59mΩ (typical) @ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- LED backlighting
- Ideal for high-frequency switching and synchronous rectification



Schematic diagram



TO-252 -2Ltop view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRRP1520K		TO-252-2L

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	14	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	68	W
Derating factor		0.45	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	65	mJ
Drain Source voltage slope, V_{DS} ≤120 V,	dv/dt	50	V/ns
Drain Source voltage slope, V_{DS} ≤120 V, I_{SD}<I_D	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Résistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	2.2	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

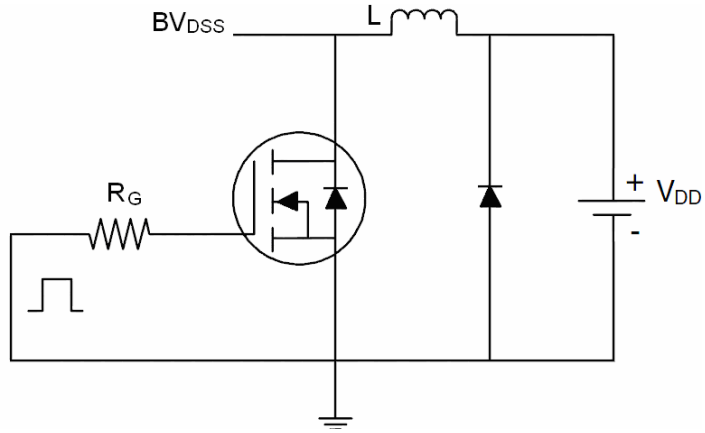
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.3	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	59	65	mΩ
Gate resistance	R_G		-	4.5	-	Ω
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=10A	15	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	-	600		PF
Output Capacitance	C_{oss}		-	74.7		PF
Reverse Transfer Capacitance	C_{rss}		-	10.8		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V, R_L=7.5Ω V_{GS}=10V,R_G=3Ω	-	9.5	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12.5	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=10A, V_{GS}=10V	-	12	-	nC
Gate-Source Charge	Q_{gs}		-	5.7	-	nC
Gate-Drain Charge	Q_{gd}		-	2.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=10A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	20	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs(Note3)	-	29	-	nS
Reverse Recovery Charge	Qrr		-	130	-	nC

Notes:

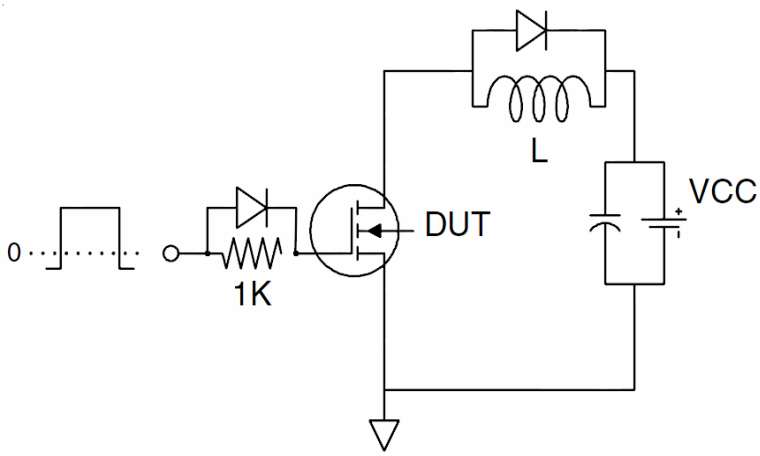
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

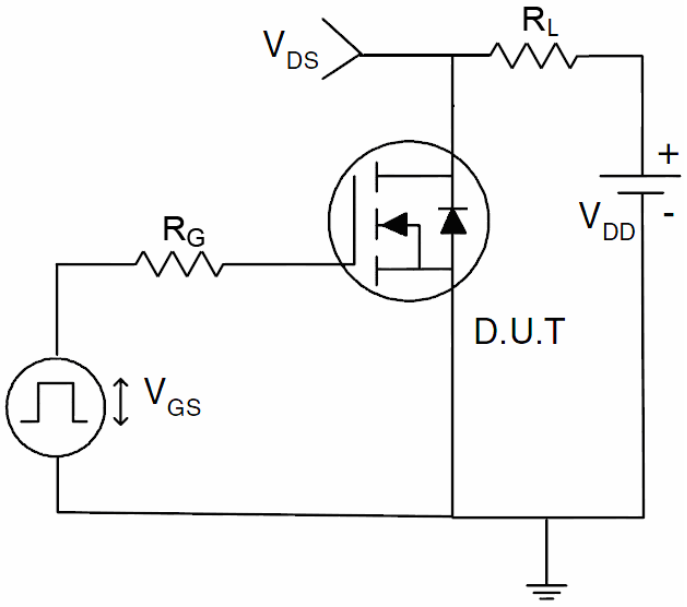
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

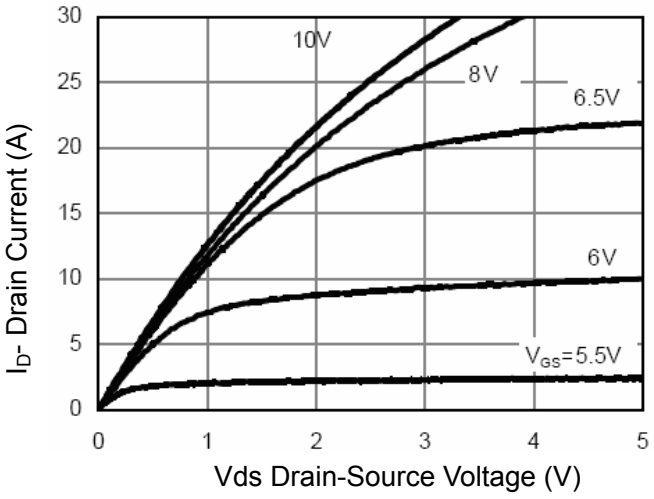


Figure 1 Output Characteristics

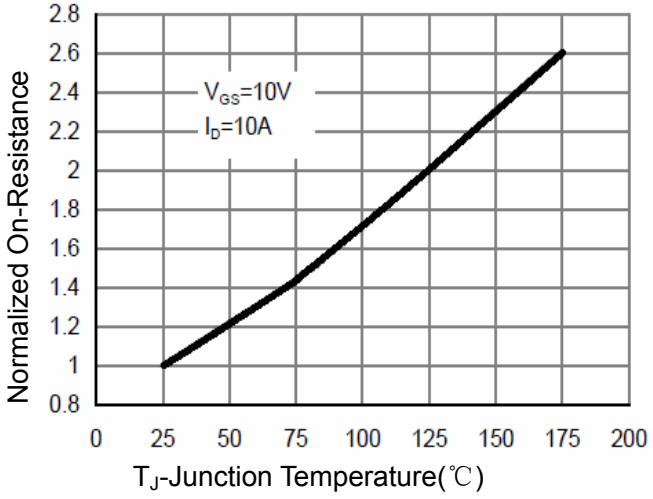


Figure 4 Rdson-Junction Temperature

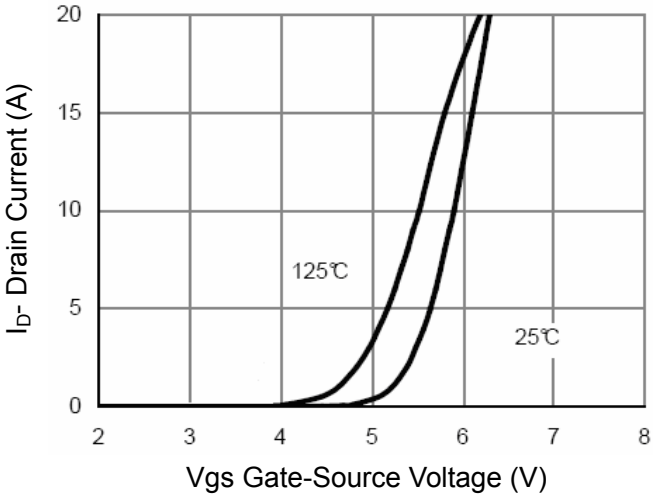


Figure 2 Transfer Characteristics

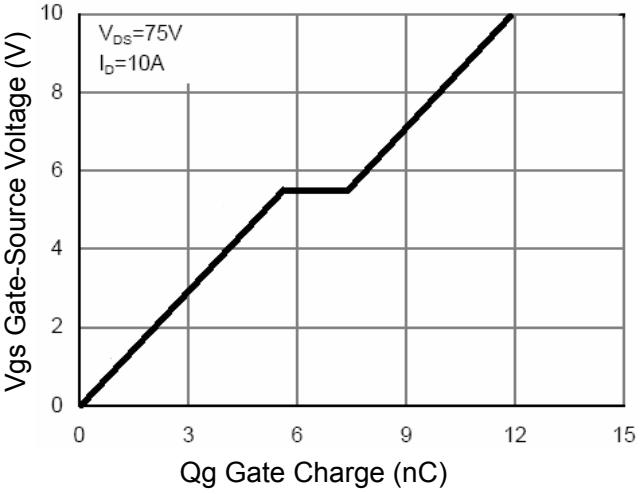


Figure 5 Gate Charge

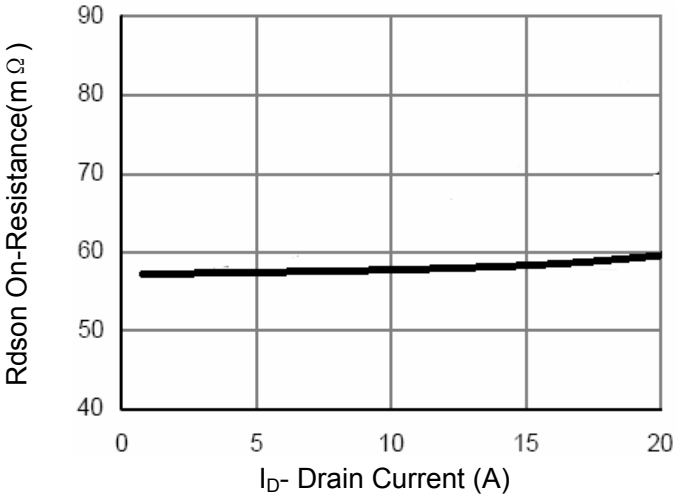


Figure 3 Rdson- Drain Current

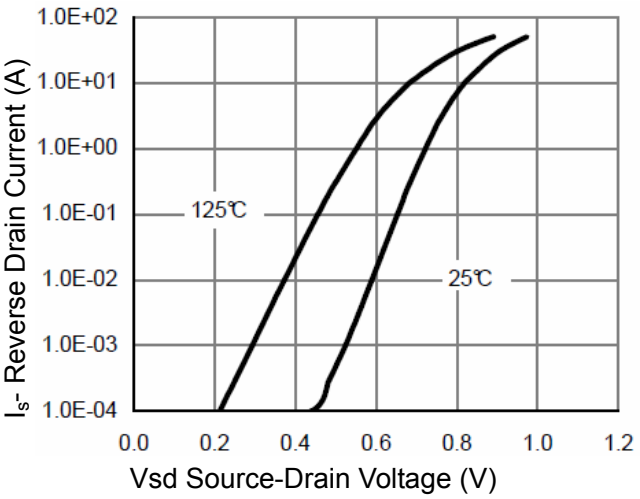


Figure 6 Source- Drain Diode Forward

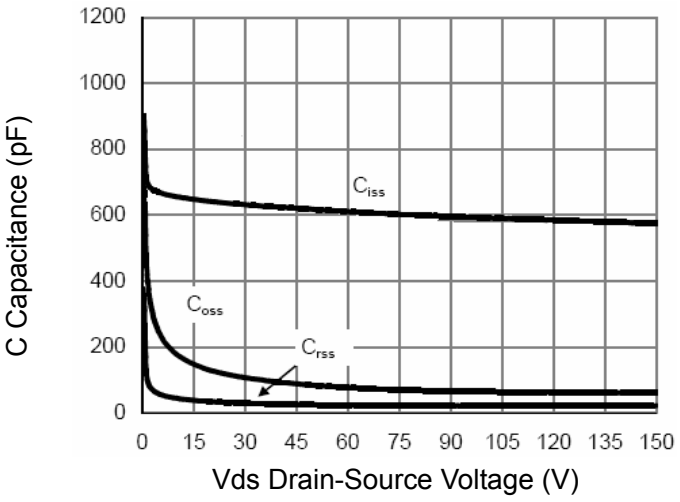


Figure 7 Capacitance vs Vds

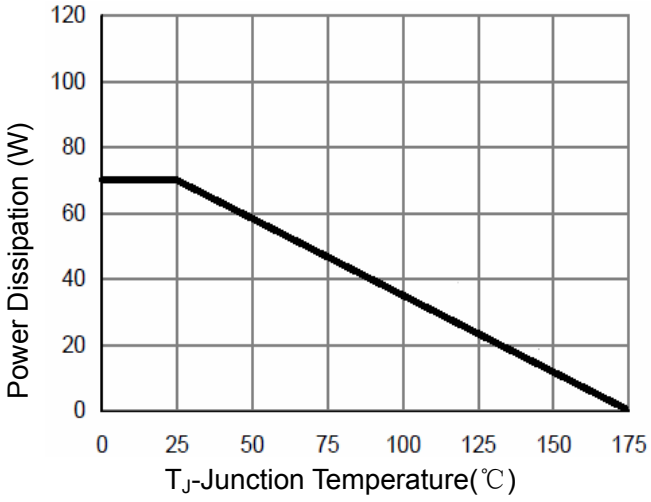


Figure 9 Power De-rating

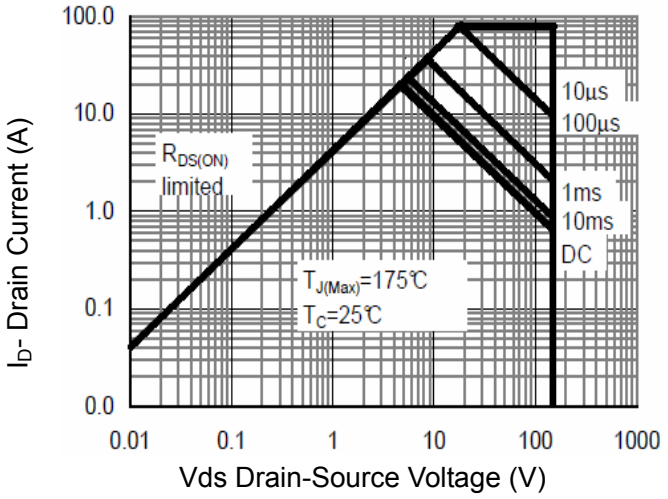


Figure 8 Safe Operation Area

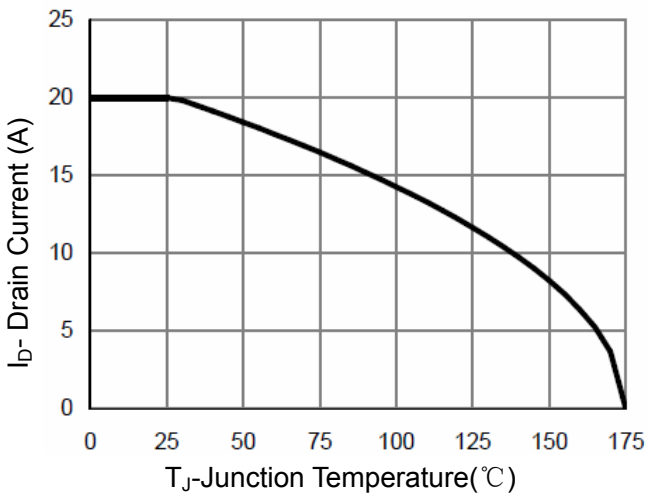


Figure 10 Current De-rating

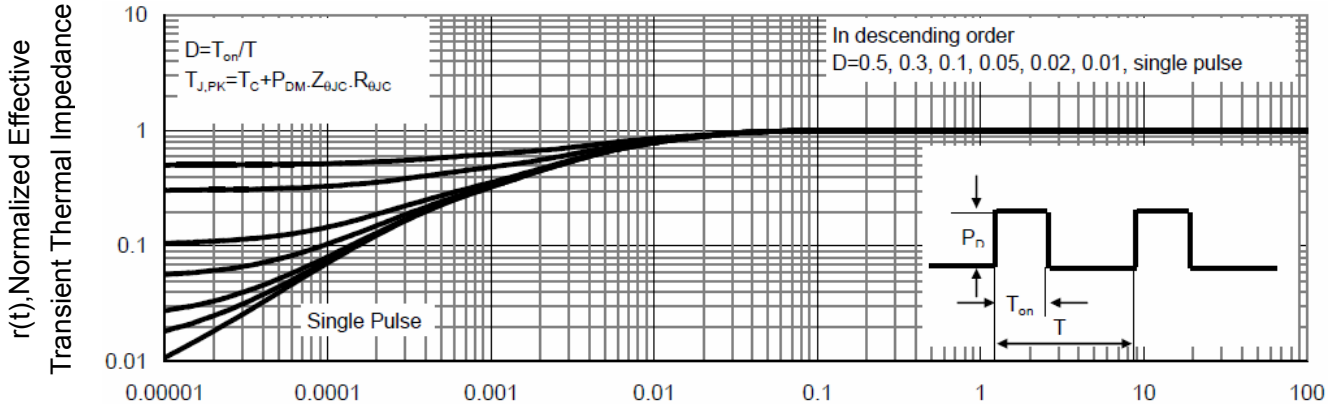
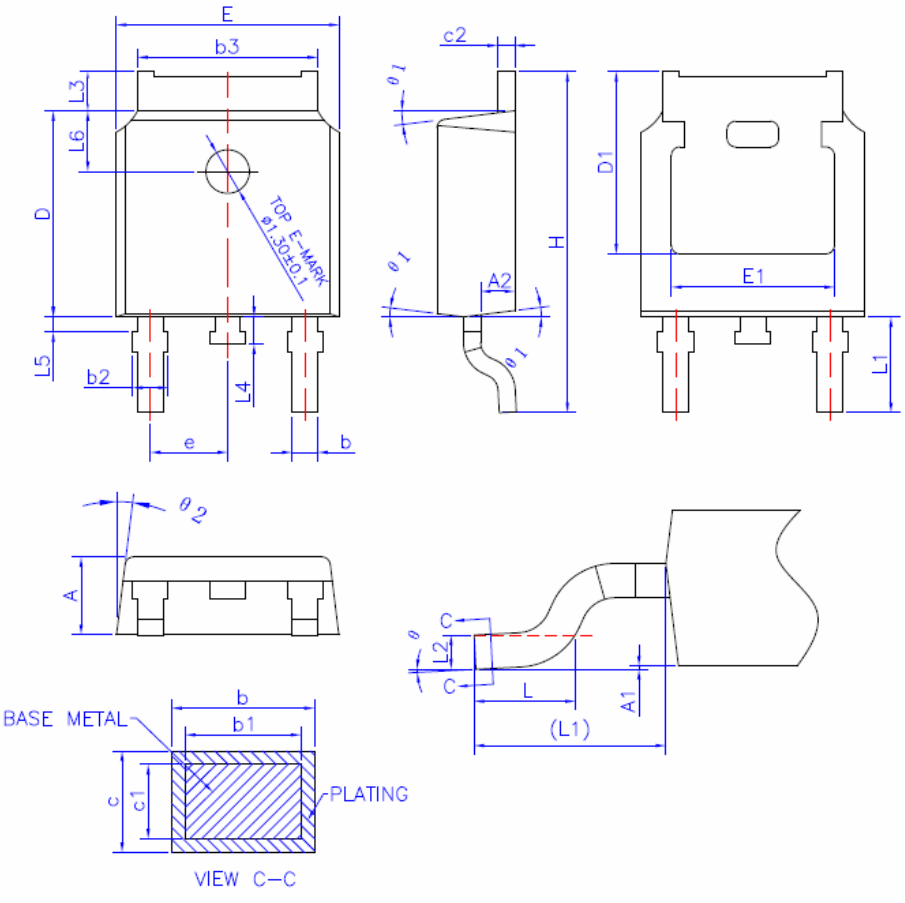


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	—	0.10
A2	0.90	1.01	1.10
b	0.72	—	0.85
b1	0.71	0.76	0.81
b2	0.72	—	0.90
b3	5.13	5.33	5.46
c	0.47	—	0.60
c1	0.46	0.51	0.56
c2	0.47	—	0.60
D	6.00	6.10	6.20
D1	5.25	—	—
E	6.50	6.60	6.70
E1	4.70	—	—
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.508 BSC		
L3	0.90	—	1.25
L4	0.60	0.80	1.00
L5	0.15	—	0.75
L6	1.80 REF		
θ	0°	—	8°
θ1	5°	7°	9°
θ2	5°	7°	9°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARED TO-252 AA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

Attention