

VCRR P-Channel Enhancement Mode Power MOSFET

Description

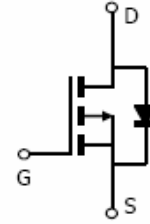
The VCRR60P40F uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

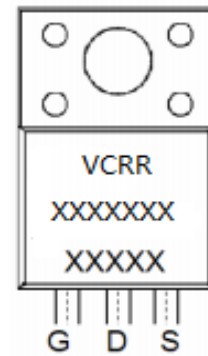
- $V_{DS} = -60V, I_D = -40A$
 $R_{DS(ON)} < 35m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

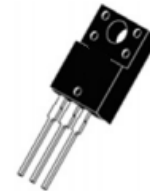
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-220F top view

Package Marking and Ordering Information

Device Marking	Device	Device Package
VCRR60P40F		TO-220F

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-40	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-28.3	A
Pulsed Drain Current ^(Note 1)	I_{DM}	160	A
Maximum Power Dissipation	P_D	37	W
Derating factor		0.25	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	168	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	4.0	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

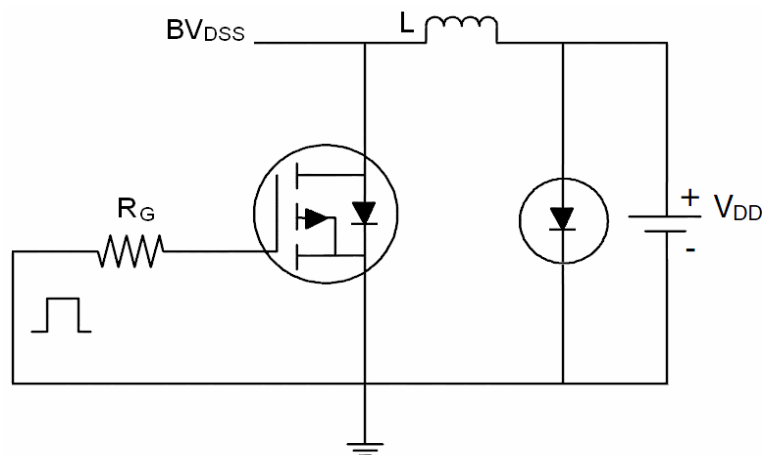
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2.0	-2.6	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	31	35	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-20A$	-	20	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{ISS}	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0MHz$	-	2049	-	PF
Output Capacitance	C_{OSS}		-	112.7	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	88.7	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, I_D=-20A$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	13	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{DS}=-30V, I_D=-20A,$ $V_{GS}=-10V$	-	35.1	-	nC
Gate-Source Charge	Q_{GS}		-	9	-	nC
Gate-Drain Charge	Q_{gd}		-	7.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-20A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	-45	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = -20A$	-	-	40	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ ^(Note 3)	-	-	70	nC

Notes:

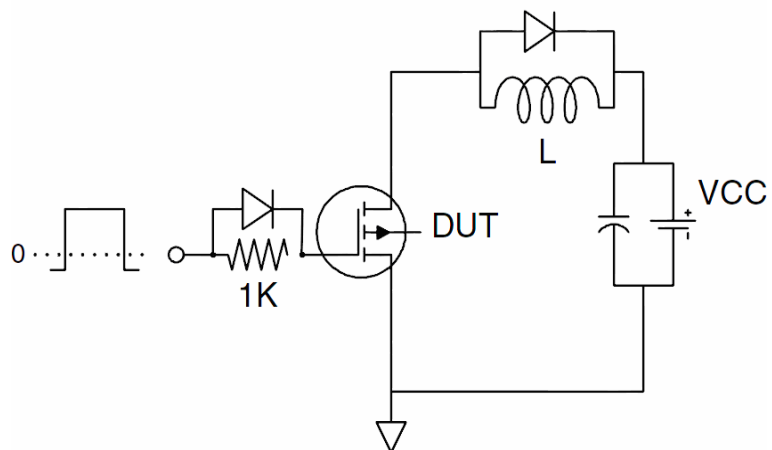
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}C, V_{DD}=-30V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

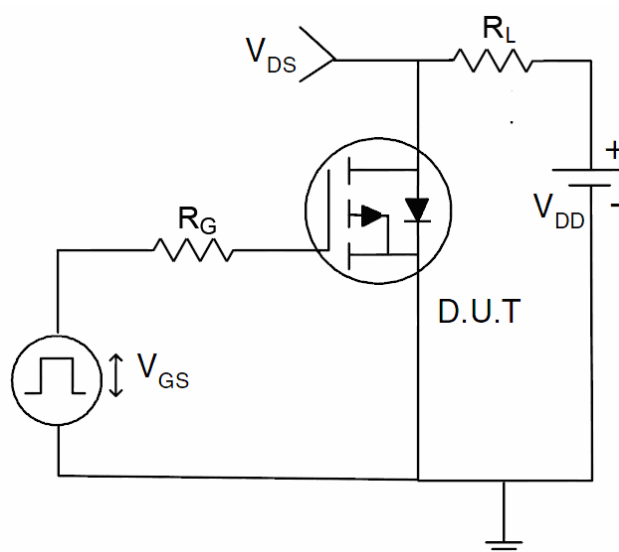
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

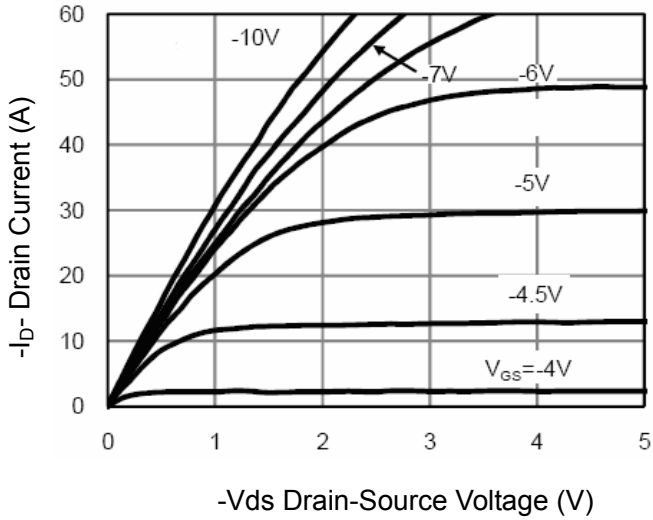


Figure 1 Output Characteristics

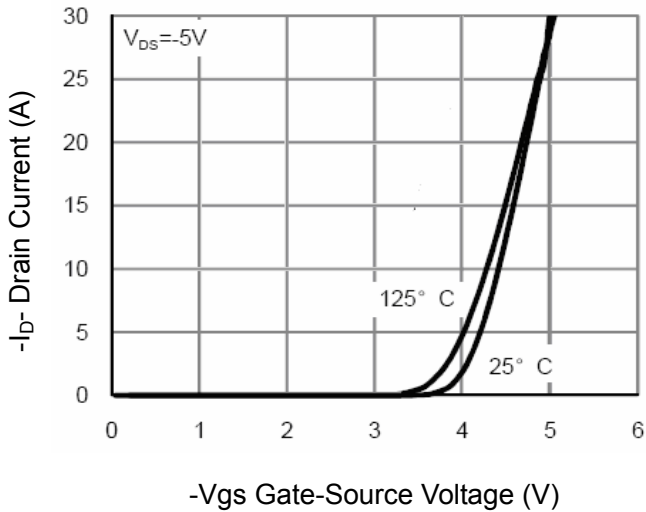


Figure 2 Transfer Characteristics

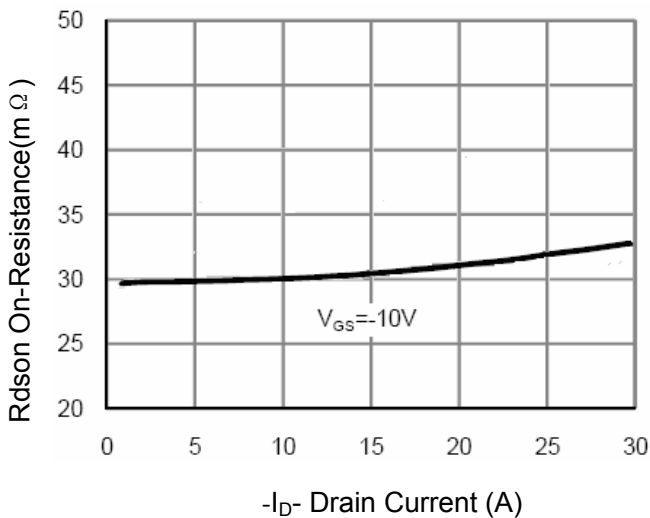


Figure 3 Rdson- Drain Current

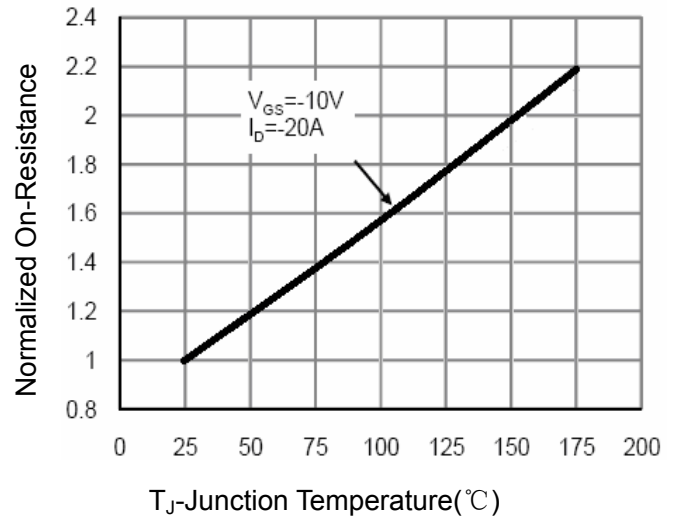


Figure 4 Rdson-Junction Temperature

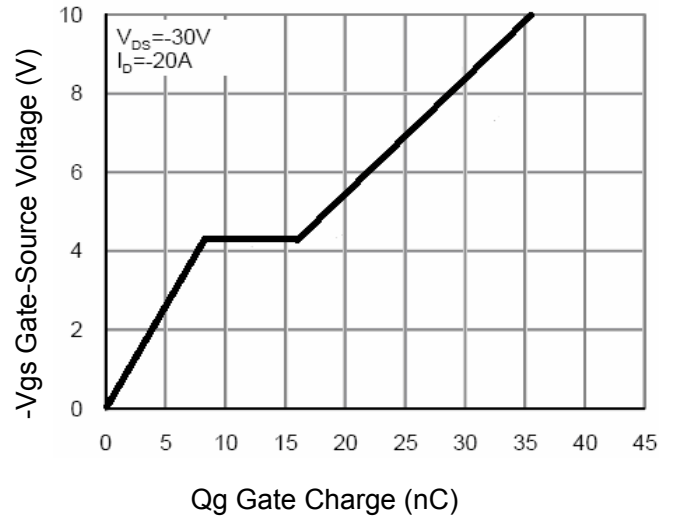


Figure 5 Gate Charge

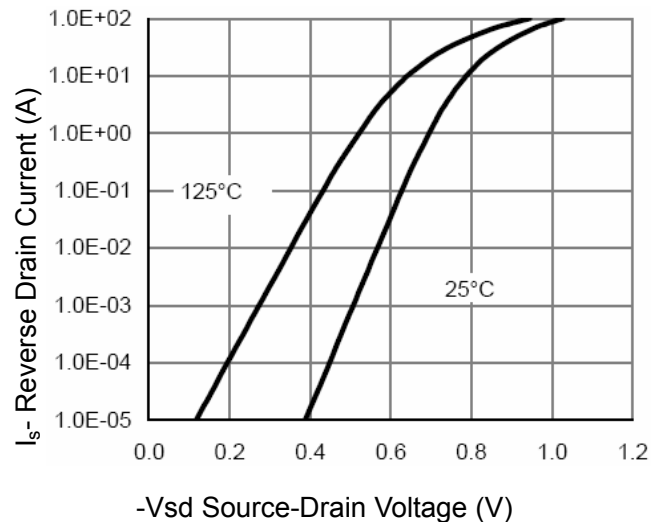
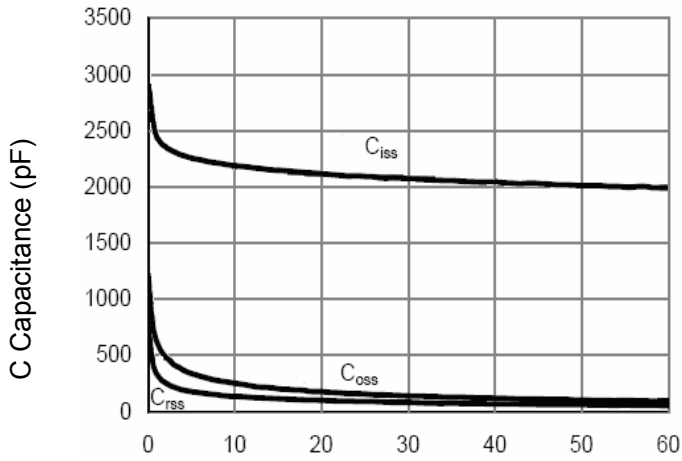
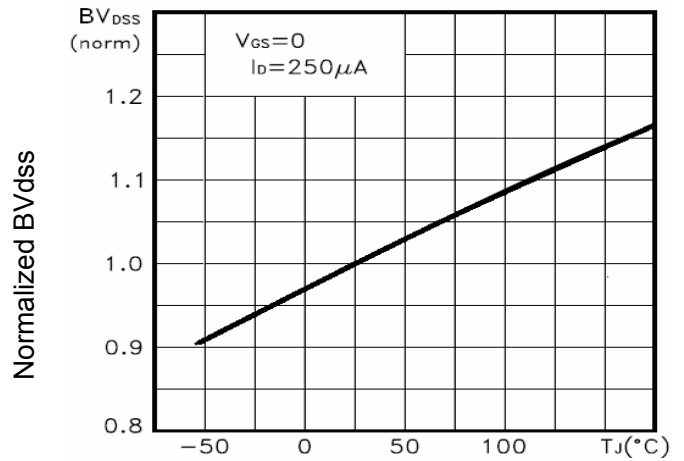


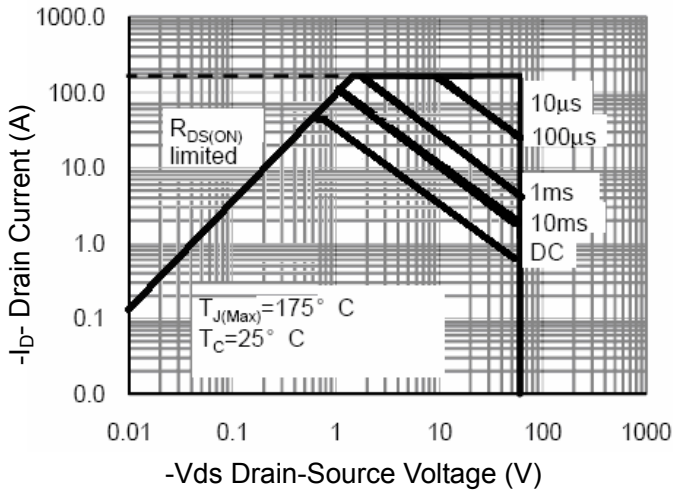
Figure 6 Source- Drain Diode Forward



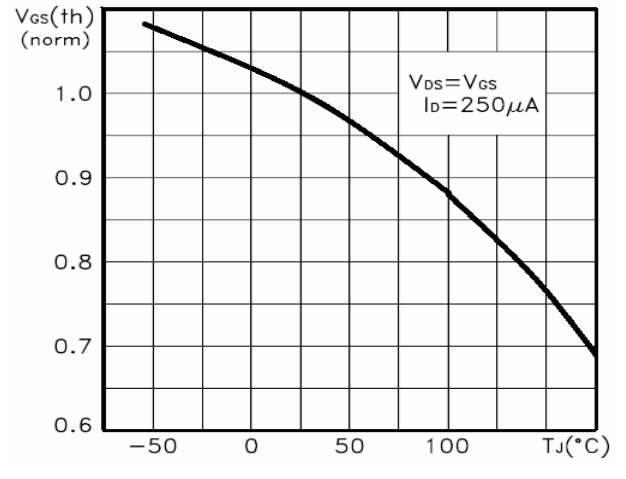
-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



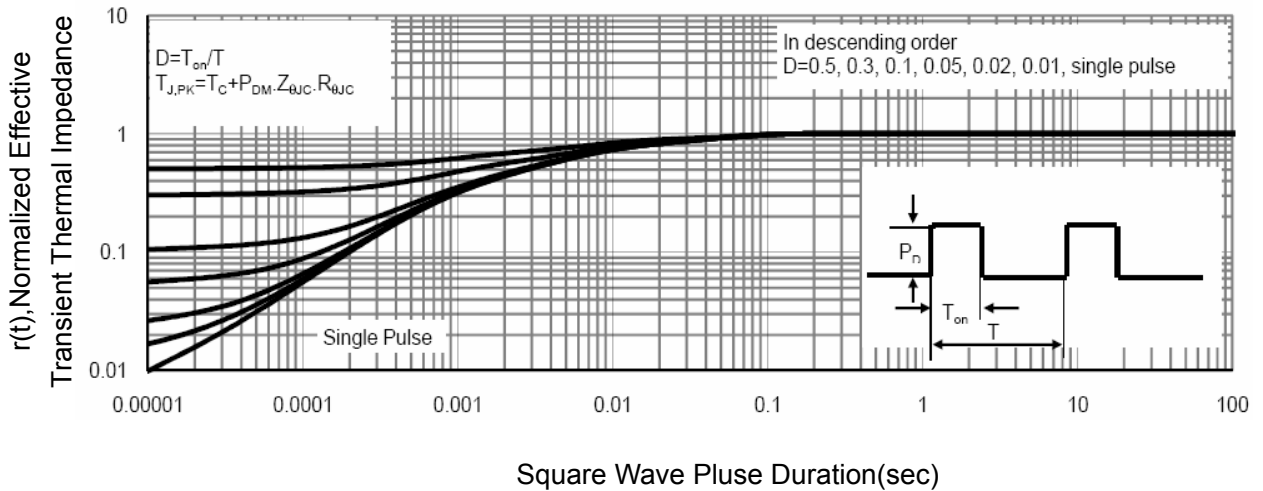
T_J -Junction Temperature ($^{\circ}\text{C}$)
Figure 9 BV_{DSS} vs Junction Temperature



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area

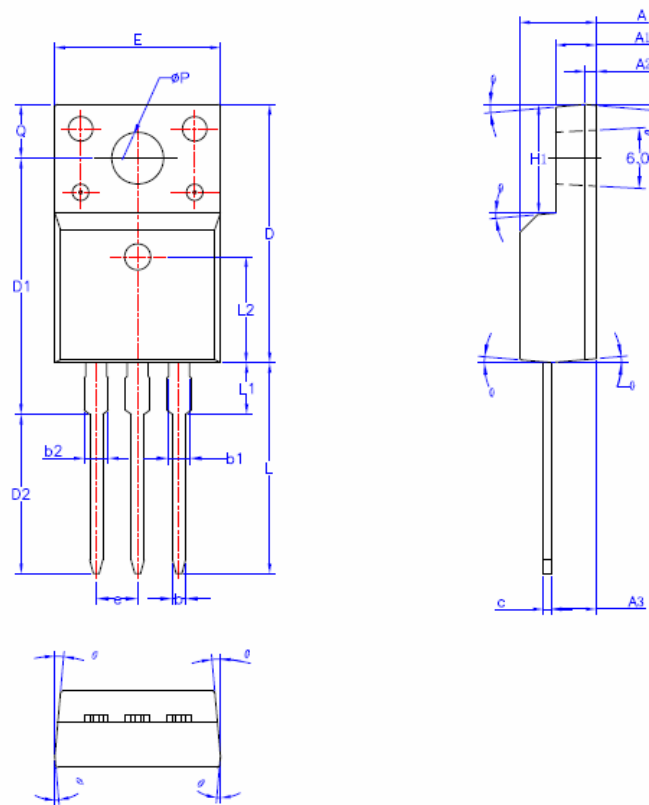


T_J -Junction Temperature($^{\circ}\text{C}$)
Figure 10 $V_{GS(th)}$ vs Junction Temperature



Square Wave Pluse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220F Package Information



SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.83
A1	2.34	2.54	2.74
A2	0.70 REF		
A3	2.56	2.76	2.93
b	0.70	—	0.90
b1	1.18	—	1.38
b2	—	—	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	9.60	9.80	10.0
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	—	—	3.50
L2	6.50REF		
ϕP	3.08	3.18	3.28
Q	3.20	—	3.40
θ	1°	3°	5°

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