

VCRR P-Channel Super Trench Power MOSFET

Description

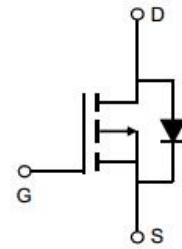
The VCRRP40P80K uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = -40V, I_D = -80A$
 $R_{DS(on)} = 7.2m\Omega$ (typical) @ $V_{GS} = -10V$
 $R_{DS(on)} = 11m\Omega$ (typical) @ $V_{GS} = -4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VCRRP40P80K		TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-80	A
Drain Current-Continuous($T_c = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	-56	A
Pulsed Drain Current	I_{DM}	-320	A
Maximum Power Dissipation	P_D	150	W
Derating factor		1	W/°C
Single pulse avalanche energy ^(Note1)	E_{AS}	500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	$^{\circ}C/W$
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Electrical Characteristics ($T_c=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.7	-2.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$	-	7.2	8.8	m Ω
		$V_{GS}=-4.5V, I_D=-20A$	-	11	14	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-20A$	-	30	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	3700	-	PF
Output Capacitance	C_{oss}		-	880	-	PF
Reverse Transfer Capacitance	C_{rss}		-	20	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, I_D=-20A$ $V_{GS}=-10V, R_G=1.6\Omega$	-	10.5	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	t_f		-	5	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-20A,$ $V_{GS}=-10V$	-	57	-	nC
Gate-Source Charge	Q_{gs}		-	9.8	-	nC
Gate-Drain Charge	Q_{gd}		-	7.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-20A$	-		-1.2	V
Diode Forward Current	I_S		-	-	-80	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = -20A$	-		24	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$	-		68	nC

Notes:

- EAS condition : $T_J=25^{\circ}C, V_{DD}=-20V, V_G=-10V, L=0.5mH, R_G=25\Omega$
- Guaranteed by design, not subject to production
- These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(MAX)=175^{\circ}C$. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

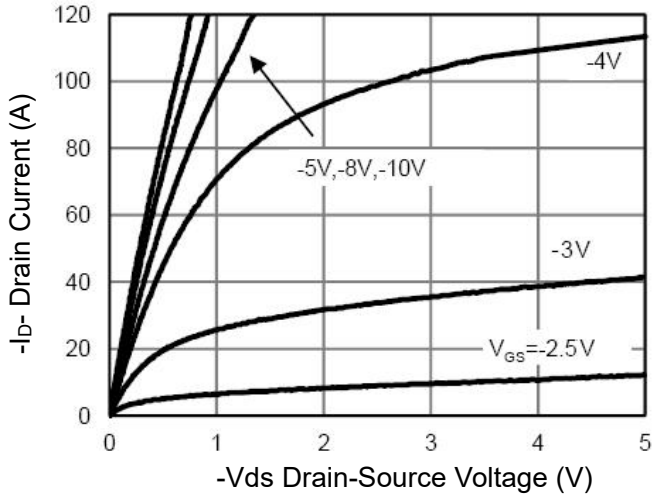


Figure 1 Output Characteristics

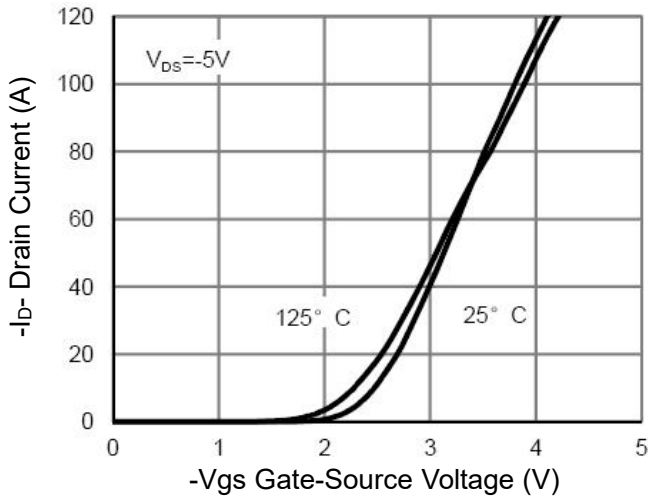


Figure 2 Transfer Characteristics

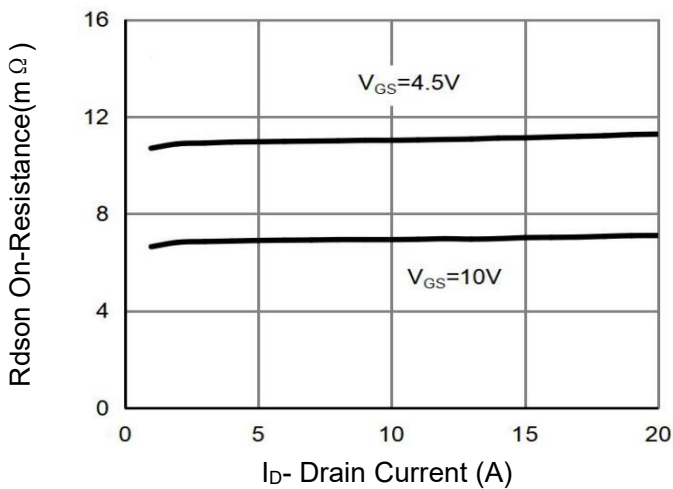


Figure 3 Rdson- Drain Current

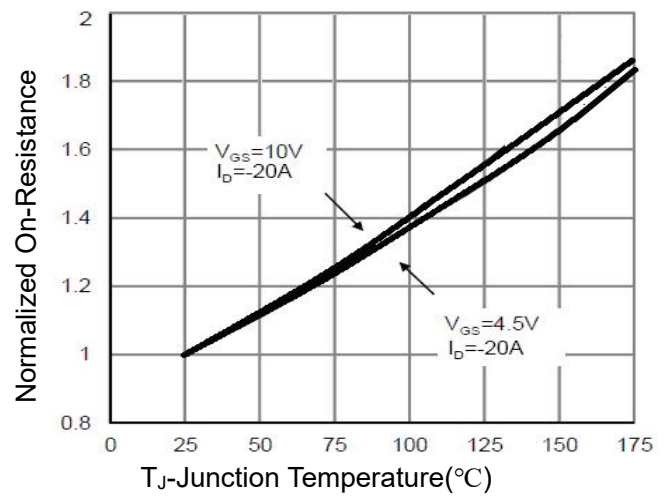


Figure 4 Rdson-Junction Temperature

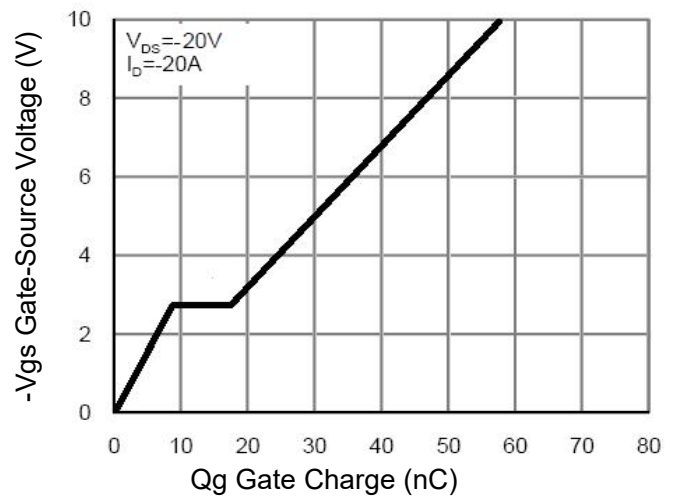


Figure 5 Gate Charge

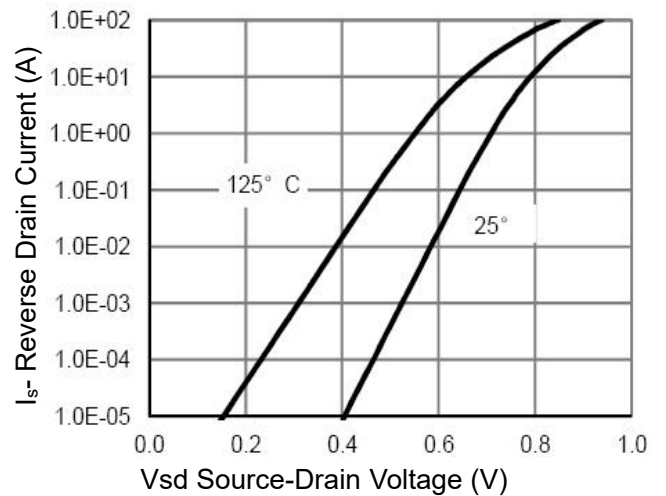


Figure 6 Source- Drain Diode Forward

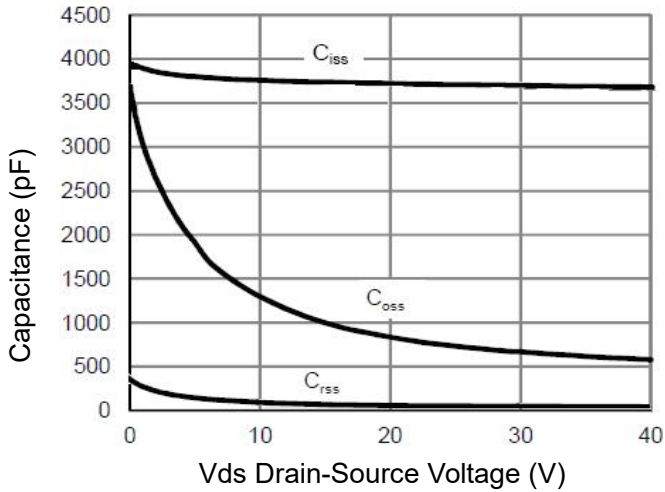


Figure 7 Capacitance vs Vds

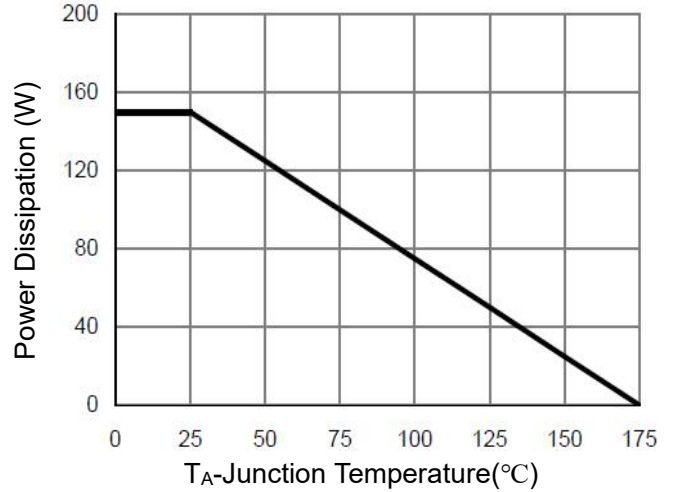


Figure 9 Power De-rating

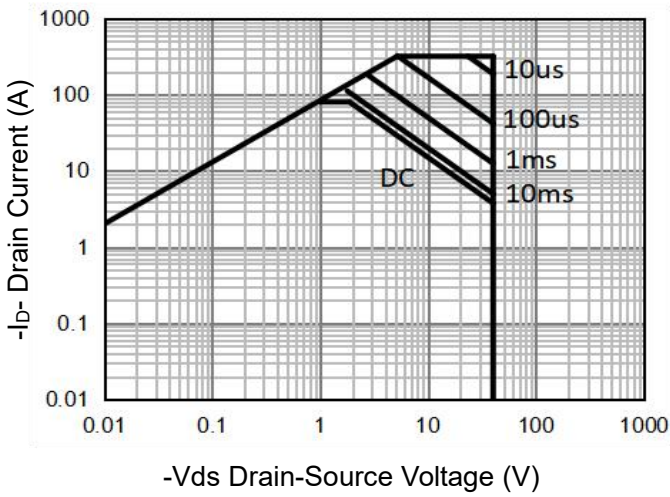


Figure 8 Safe Operation Area (Note 3)

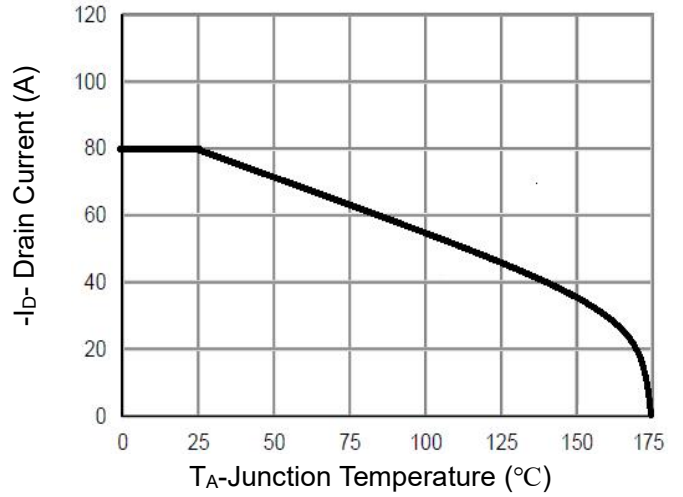


Figure 10 Current De-rating

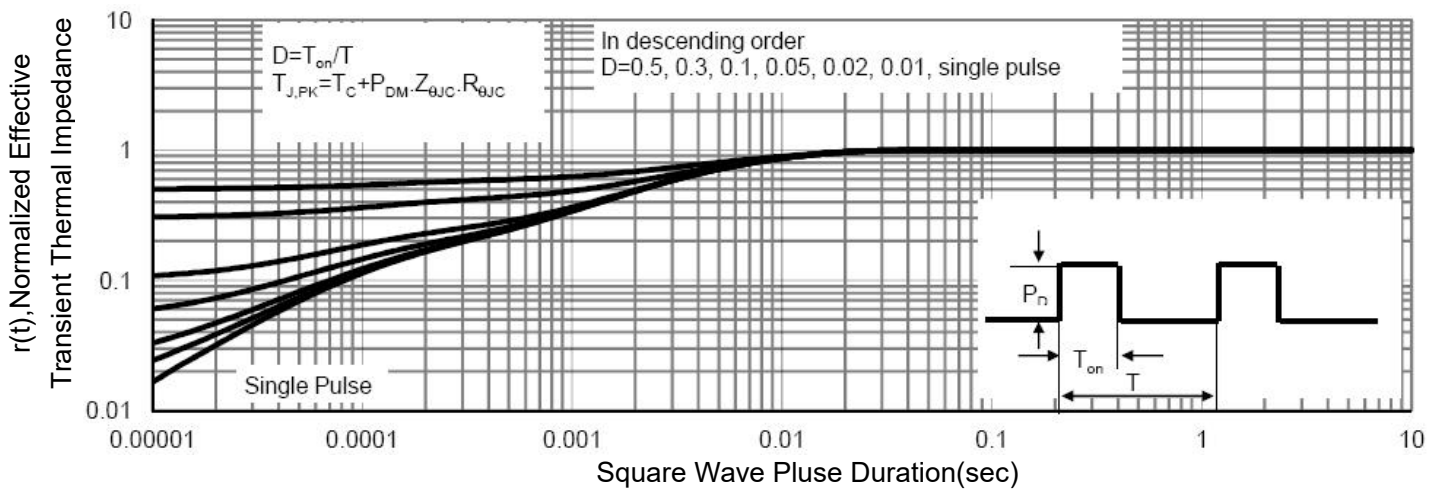
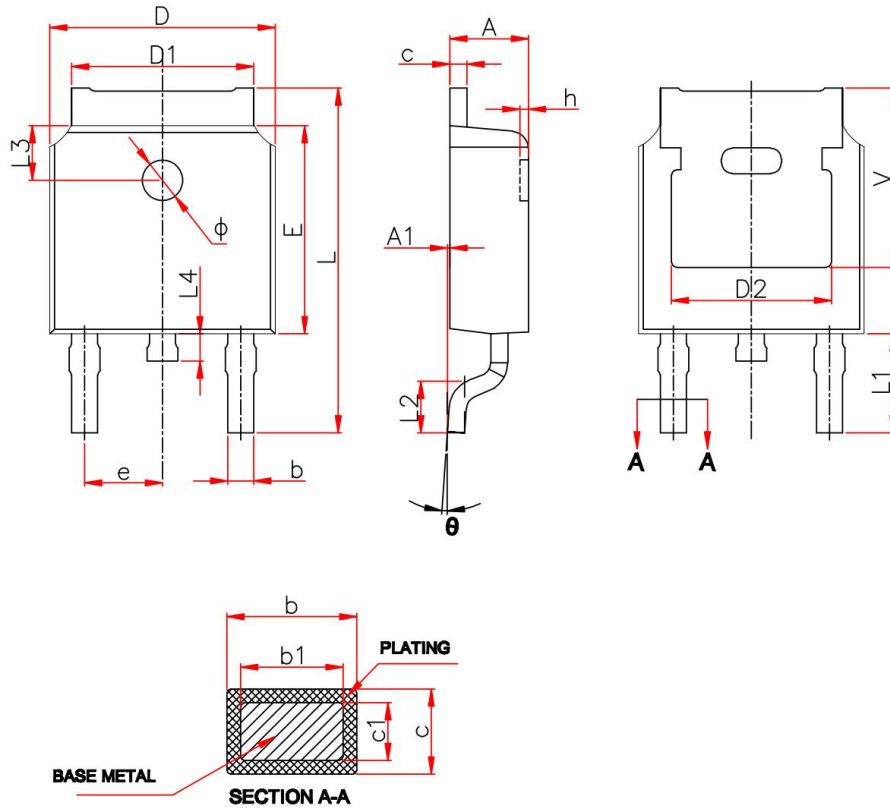


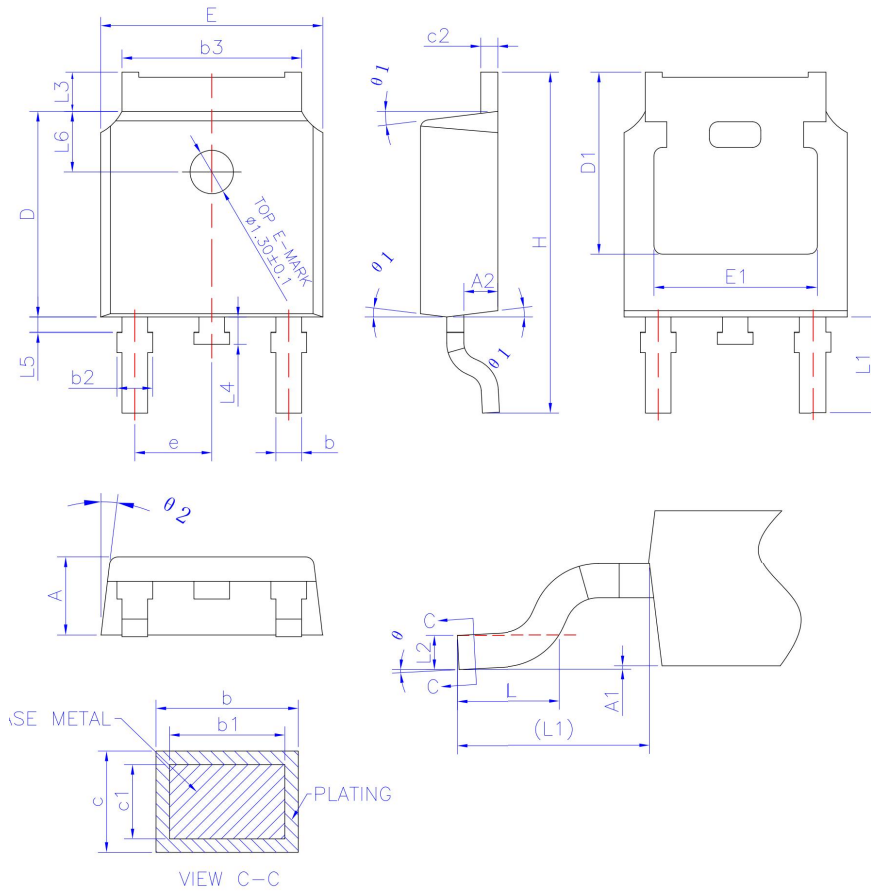
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L(E) Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
ϕ	1.10	1.30
θ	0°	8°

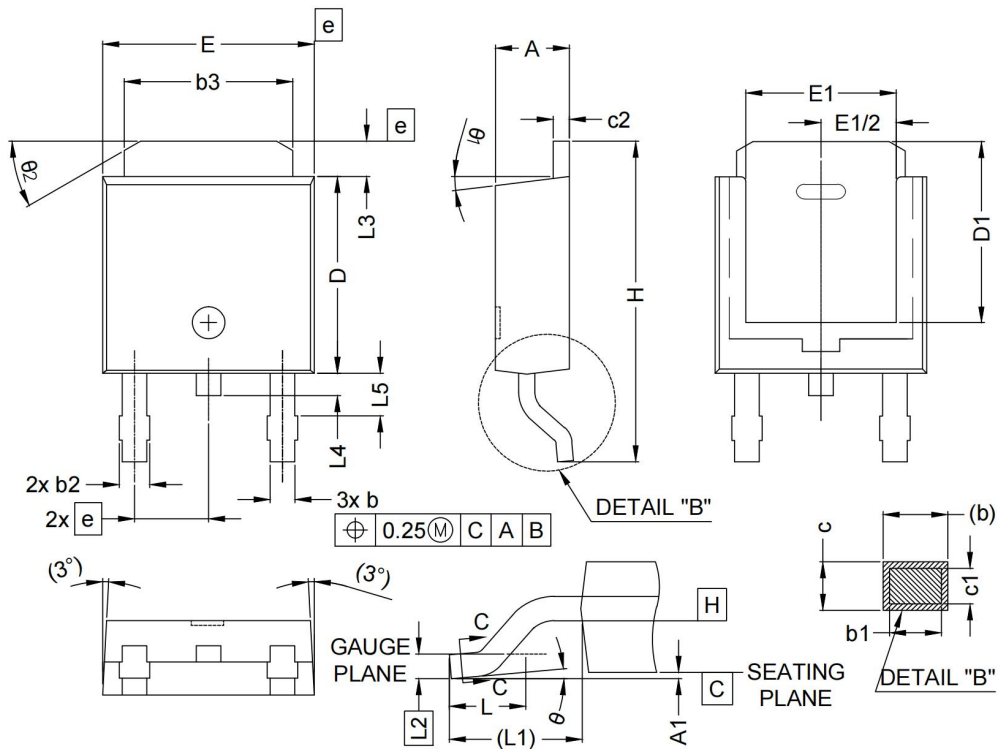
TO-252-2L(P) Package Information



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	---	0.10
A2	0.90	1.01	1.10
b	0.72	---	0.85
b1	0.71	0.76	0.81
b2	0.72	---	0.90
b3	5.13	5.33	5.46
c	0.47	---	0.60
c1	0.46	0.51	0.56
c2	0.47	---	0.60
D	6.00	6.10	6.20
D1	5.25	---	---
E	6.50	6.60	6.70
E1	4.70	---	---
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.508 BSC		
L3	0.90	---	1.25
L4	0.60	0.80	1.00
L5	0.15	---	0.75
L6	1.80 REF		
theta	0°	---	8°
theta1	5°	7°	9°
theta2	5°	7°	9°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD
TO-252 AA DO NOT INCLUDE MOLD FLASH OR
PROTRUSIONS

TO-252-2L(B) Package Information



SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	θ_1	0°	15°
A1	-	0.13	E1	4.32	-	θ_2	25°	35°
b	0.65	0.89	e	2.29 BSC				
b1	0.64	0.79	H	9.94	10.34			
b2	0.76	1.13	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.46	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.14	1.49			
D1	5.21	-	θ	0°	10°			

NOTE ; 1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
 2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
 3.0 HEAT SINK SIDE FLASH IS MAX. 0.8mm.
 4.0 RADIUS ON TERMINAL IS OPTIONAL.

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