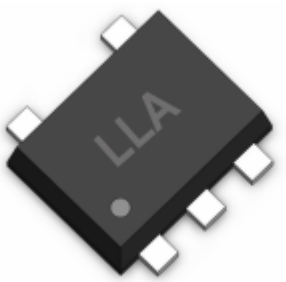
QIAOXIN SEMI CONDUCTOR

Transient Voltage Suppressors for ESD Protection

ESD3.3V55T-4SLC

Description

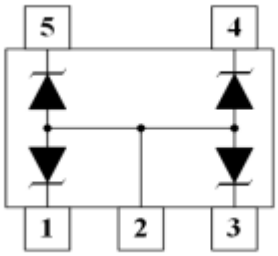
The ESD3.3V55T-4SLC is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium.



Feature

- 68 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects Four High Speed lines
- Low clamping voltage
- Working voltage : 3.3V
- Low leakage current
- IEC61000-4-2 (ESD) ±20kV (air), ±15kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ηs)
- IEC61000-4-5 (LIGHTING) 4.5A (8/20 μ s)

Functional Diagram



Applicantions

- Digital Visual Interface
- USB 3.0 / 3.1 Ports
- LCD TV
- Serial ATA
- Firewire Ports
- Customer Premise Equipment
- HDMI 1.4 / 2.0 Ports

Mechanical Data

- JEDEC SOT-553 Package
- Molding Compound Flammability Rating : UL 94V-O
- Weight 3.0 Milligrams (Approximate)
- Lead Finish : Lead Free

Mechanical Characteristics

Symbol	Parameter	Value	Units
Ppp	Peak Pulse Power (tp=8/20μs waveform)	68	Watts
TL	Lead Soldering Temperature	260 (10 sec.)	°C
T_{STG}	Storage Temperature Range	-55 to +150	°C
T_J	Operating Junction Temperature Range	-40 to +125	°C

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Electrical Characteristics(@25℃ Unless Otherwise Specifiled)

Characteristics	Symbol	Test Conditions	Min.	Type	Max.	Unit
Reverse Working Voltage	VRWM		--	-	3.3	V
Reverse Breakdown Voltage	VBR	IT=1mA;	6	7.5	9	V
Reverse Leakage Current	IR	VRWM =3.3V, T=25°C;	--	--	0.1	μA
Positive Clamping Voltage	VC	IPP =1A, TP =8/20μs;	--	--	8	V
Junction Capacitance	CJ	VR = 0V, f = 1MHz;	--	0.4	--	pF

Characteristics Curves

Fig1: 8/20μs Pulse Waveform

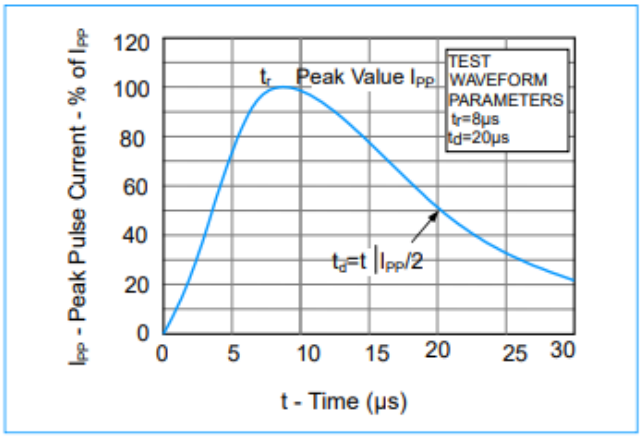


Fig2. Power Rating Derating Curve

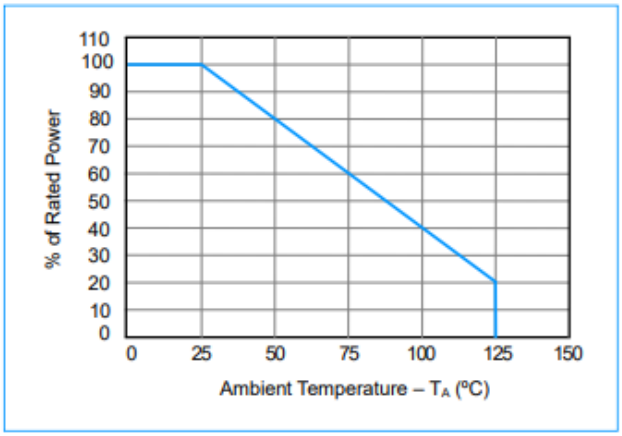


Fig3. ESD Pulse Waveform(according to IEC61000-4-2)

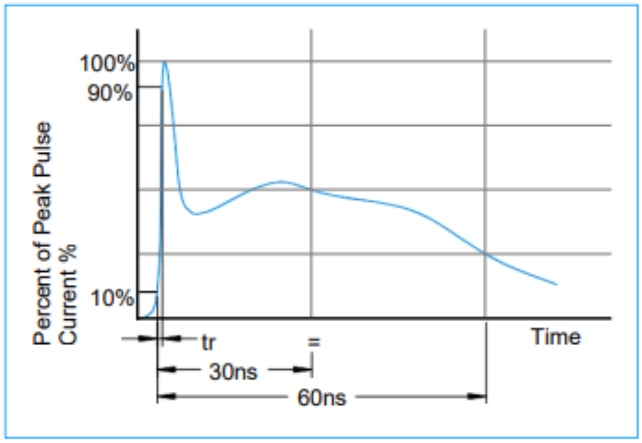


Fig4. Clamping Voltage vs. Peak Pulse Current (TLP)

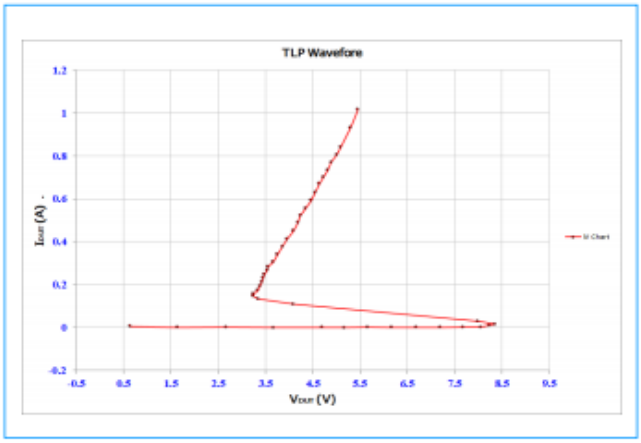


Fig5. Typic Breakdown Voltage vs. Temperature

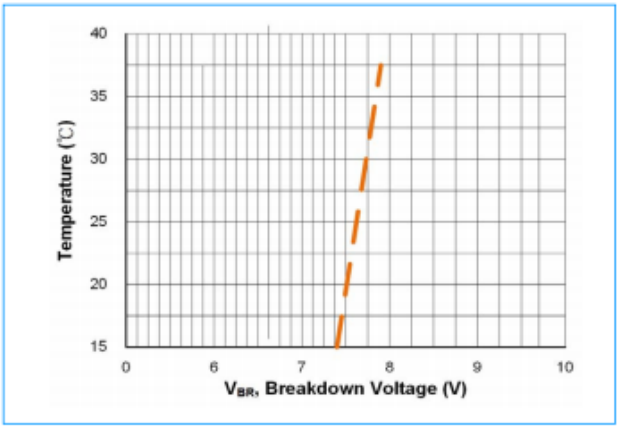


Fig6. Typic Reverse Current vs. Temperature

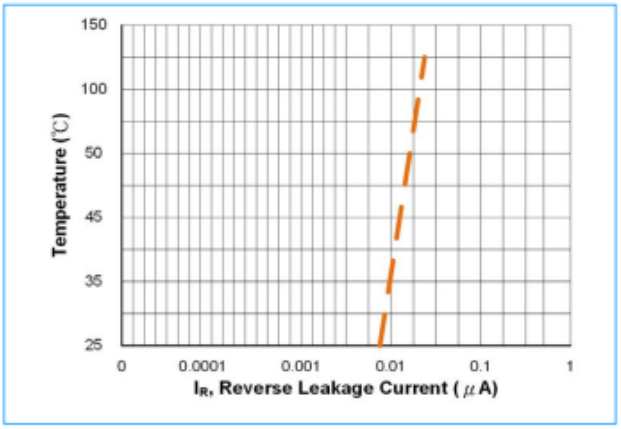
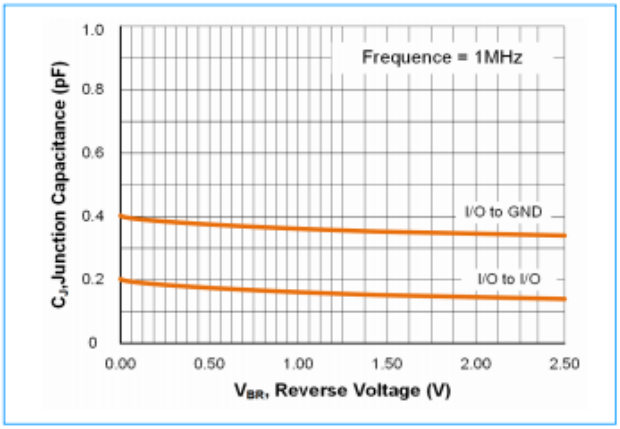
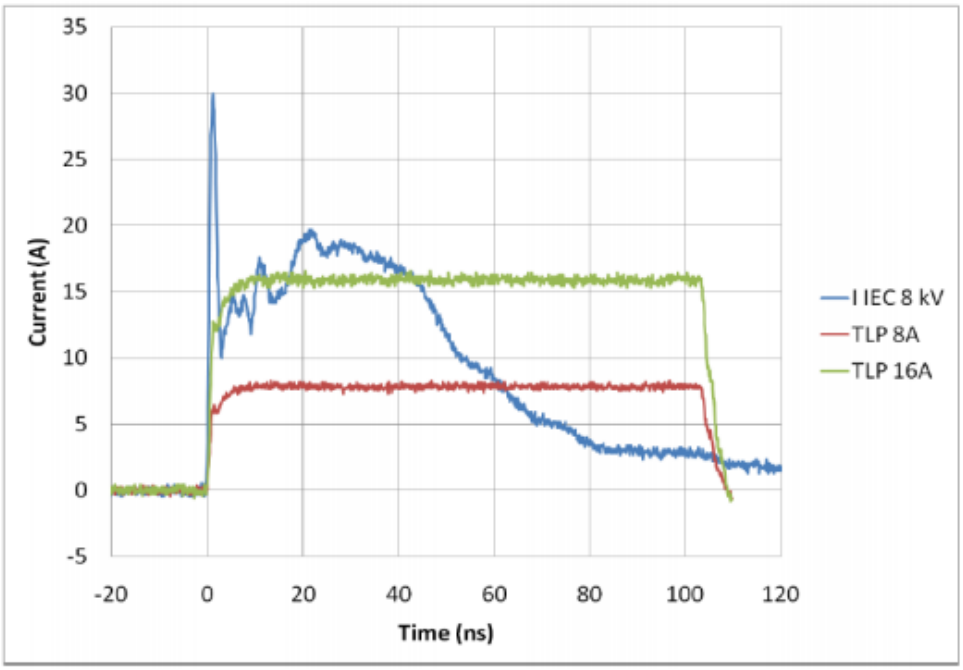


Fig7. Typic Capacitance vs. Reverse Voltage



Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I–V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 kV IEC 61000–4–2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000–4–2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for SDI Technology's protection products.



Comparison Between 8 kV IEC 61000–4–2 and 8 A and 16 A TLP Waveforms

Comparison of a Current Waveform of IEC 61000–4–2w ith TLP Pulses at 8 and 16 A.
The IEC 61000–4–2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope.
The points A, B, and C show the points on the aveforms specified in IEC 61000–4–2.
Transmission Line Pulse (TLP) Version.

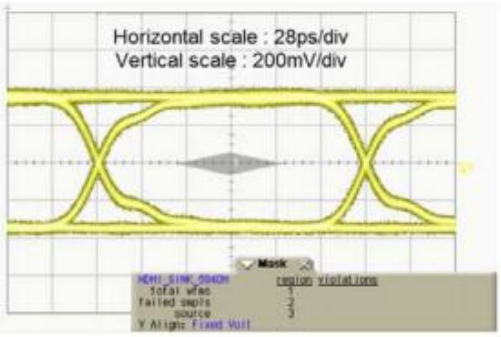


Fig. 8.1. @HDMI 2.0 mask at 5.94 Gbps per channel (Without Component)

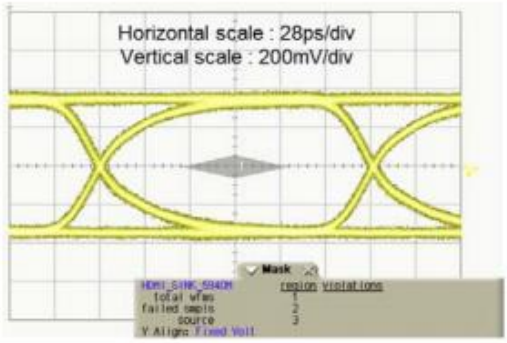


Fig. 8.2. @HDMI 2.0 mask at 5.94 Gbps per channel (With Component)

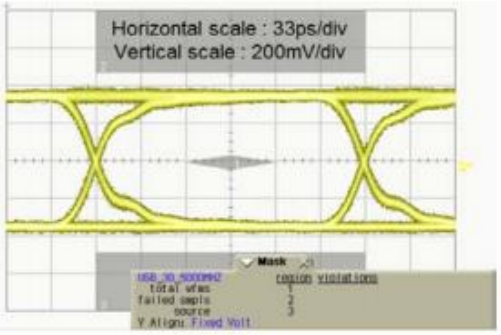


Fig. 8.3. @USB 3.0 mask at 5.0 Gbps per channel (Without Component)

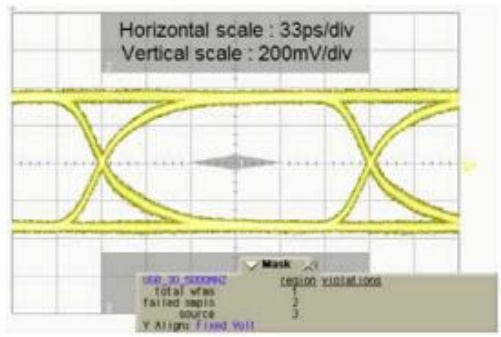


Fig. 8.4. @USB 3.0 mask at 5.0 Gbps per channel (With Component)

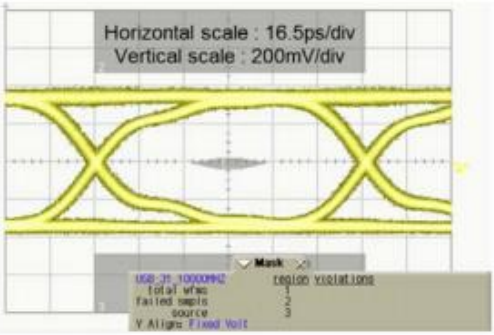


Fig. 8.5. @USB 3.1 mask at 10.0 Gbps per channel (Without Component)

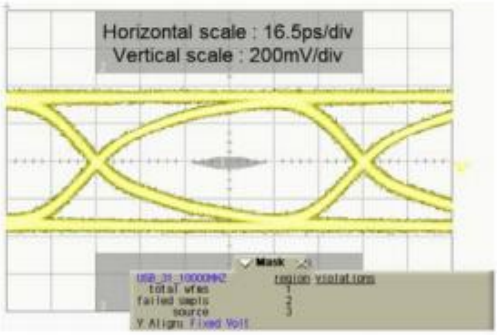


Fig. 8.6. @USB 3.1 mask at 10.0 Gbps per channel (With Component)

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

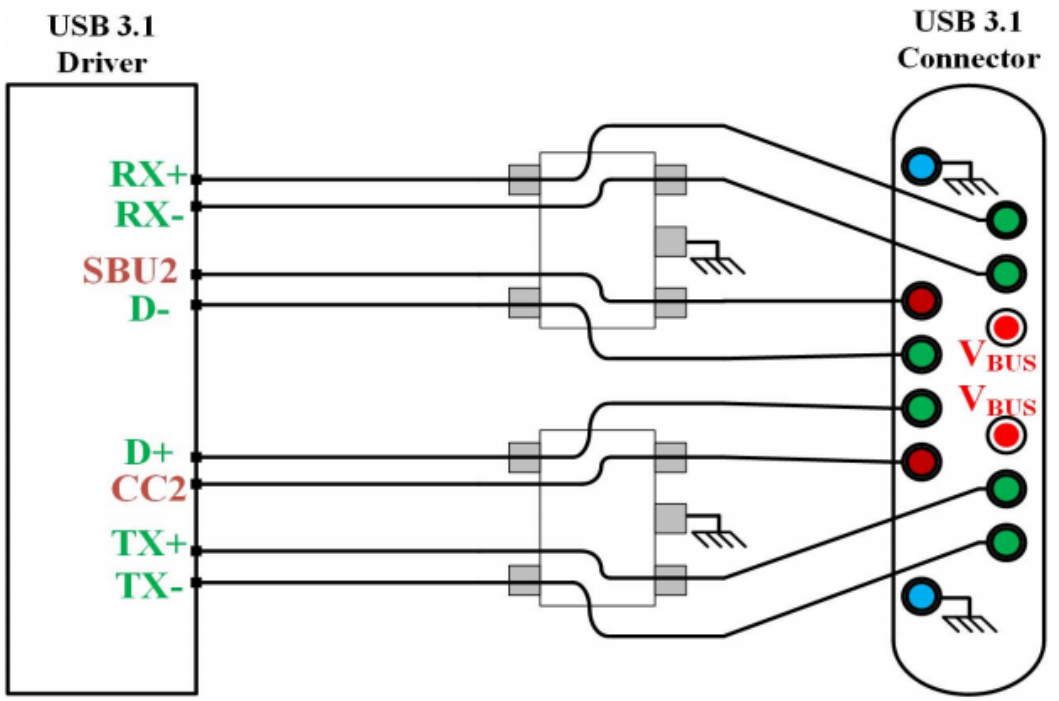
1.1. In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

2.1. Use curved traces when possible to avoid unwanted reflections.

2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



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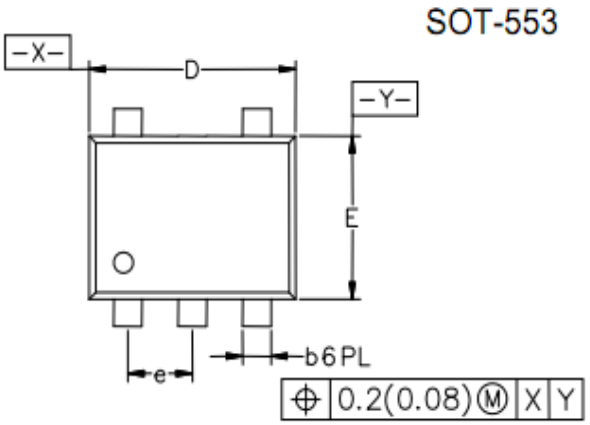
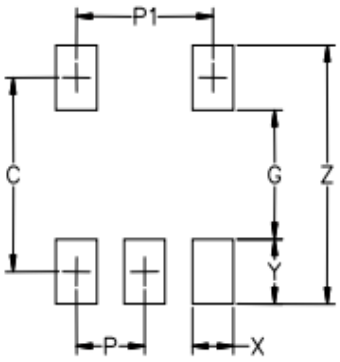
SOT-553 Package Outline &Dimensions



Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.020	0.021	0.023	0.50	0.55	0.60
b	0.007	0.009	0.011	0.17	0.22	0.27
C	0.003	0.005	0.007	0.08	0.12	0.18
D	0.059	0.062	0.066	1.50	1.60	1.70
E	0.043	0.047	0.051	1.10	1.20	1.30
e	0.02BSC			0.50BSC		
L	0.004	0.008	0.012	0.10	0.20	0.30
HE	0.059	0.062	0.067	1.50	1.60	1.70

Soldering Footprint



Symbol	Inches	Millimeters
C	0.0531	1.35
G	0.0354	0.90
P	0.0197	0.50
P1	0.0394	1.00
X	0.0118	0.30
Y	0.0177	0.45
Z	0.0709	1.80

Ordering Information

Device	Marking	Package	Quantity	Reel Size
ESD3.3V-55T-4SLC	LLA	SOT-553	3,000pcs/Reel	7 inch